

662T-M

Rev: 1.0

Page Index =====

Revision History :


Ver A: 1. First Realse


- Ver 1.0:
1. Remove RTL8201CL Co-lay
 2. Change PWM Spec
 3. Single Fuse For Each USB Port
 4. Add SLP_S5- Signal For DIMM Power Control
 5. FIX GLED GPIO Selection To GPIO14
 6. Reverse GPIO 11 For Lan-Phy AC131 Reset
 7. Modify DIMM SPD Power BY VCC3
 8. Change LAN ESD Part From BAV99 to SRV05
 9. Modify ICSPR600 Vttpwr GD By ISL6312 PWGD
and Spilit NB TESTMODE2 Circuit
 10. Modify 3-Pin Fan Control Transistor To TO-251

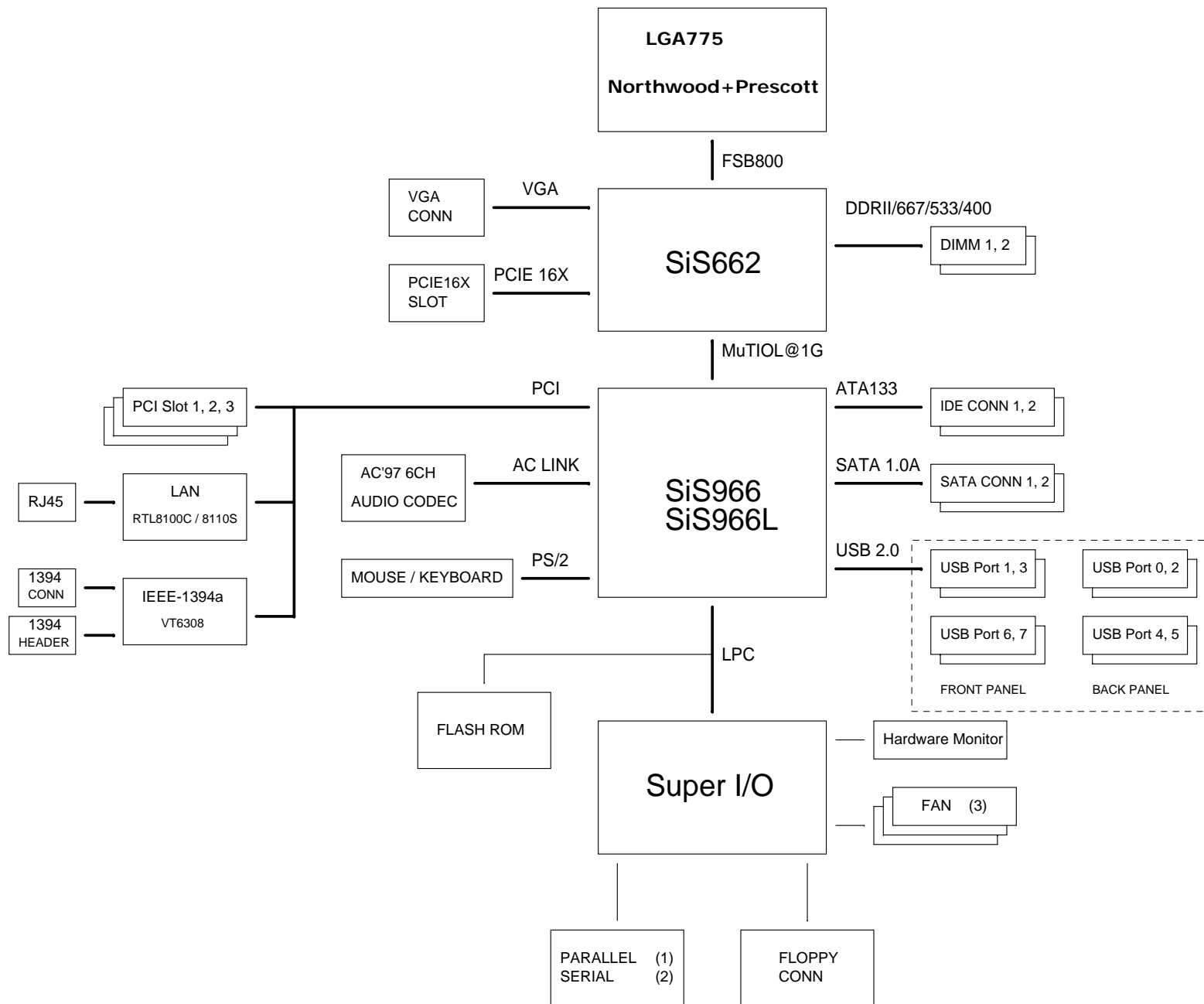
1. Cover Sheet
2. Block Diagram
3. Clock & Power Distribution
4. Socket LGA775-1
5. Socket LGA775-2
6. Socket LGA775-3
7. SiS649-1 (HOST / PCI-EX)
8. SiS649-2 (Memory)
9. SiS649-3 (LINK)
10. SiS649-4 (Power)
11. SiS965-1 (PCI / IDE / HyperZip)
12. SiS965-2 (Misc. Signals)
13. SiS965-3 (USB)
14. SiS965-4 (Power)
15. Main Clock
16. Clock Buffer
17. DDR DIMMII 1, 2
18. DDRII Termination
19. PCI-EXPRESS *16
20. VGA / IDE Connectors
21. USB Connector
22. PCI Slot1, 2
23. PCI3 / LANPHY
24. PCILAN
25. IEEE1394a
26. Audio Codec
27. Audio Interface
28. Super I/O
29. KB/MS/ROM/FDC/IR
30. COM 1,2 / LPT
31. HM/FAN/RING/LPC
32. Voltage Regulator
33. DUAL 5V, 3V& SB Regulator
34. VRD10 (CPU Vcore)
35. ATX / Panel / RTC
36. BOM and GPIO Attention

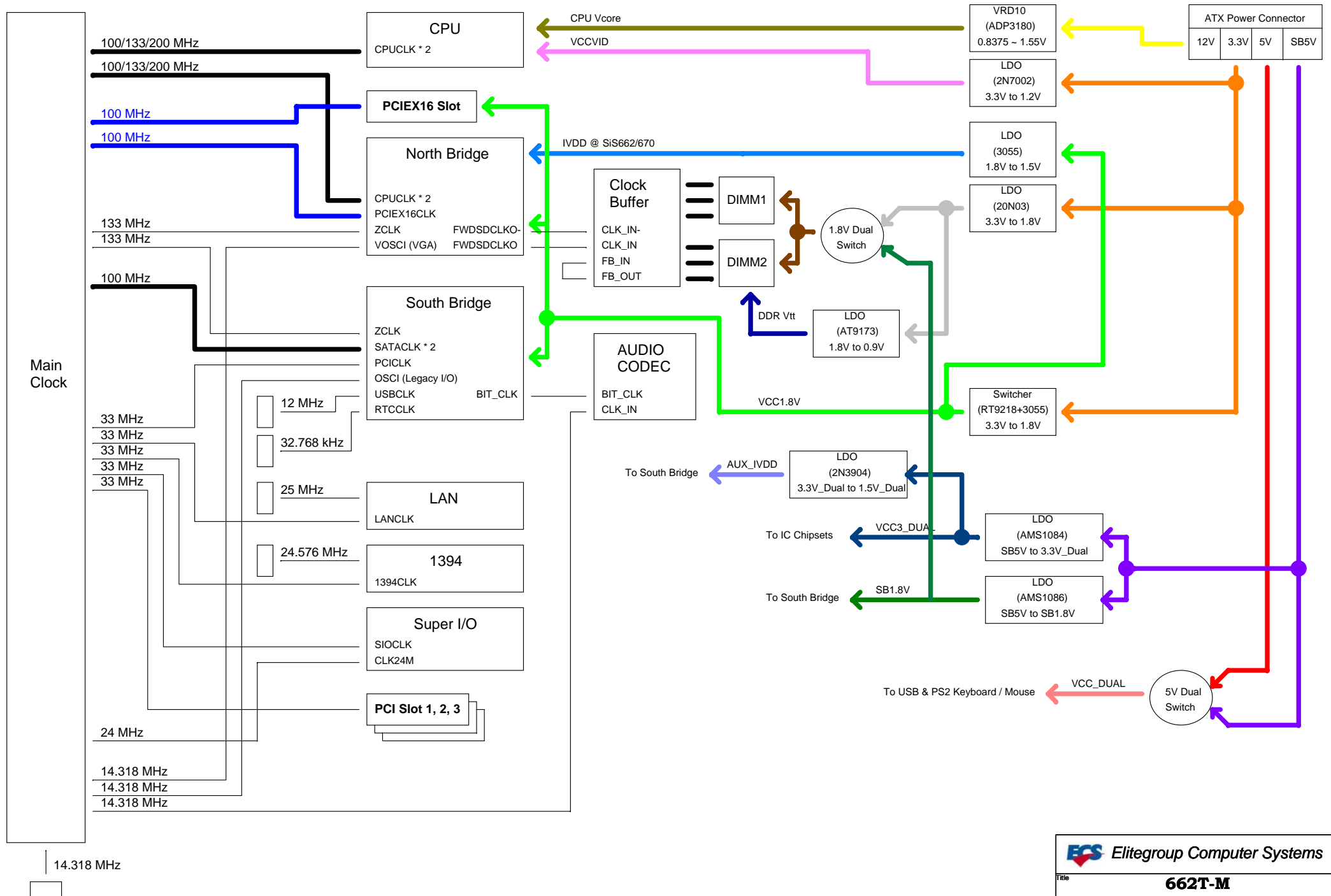
Update note:

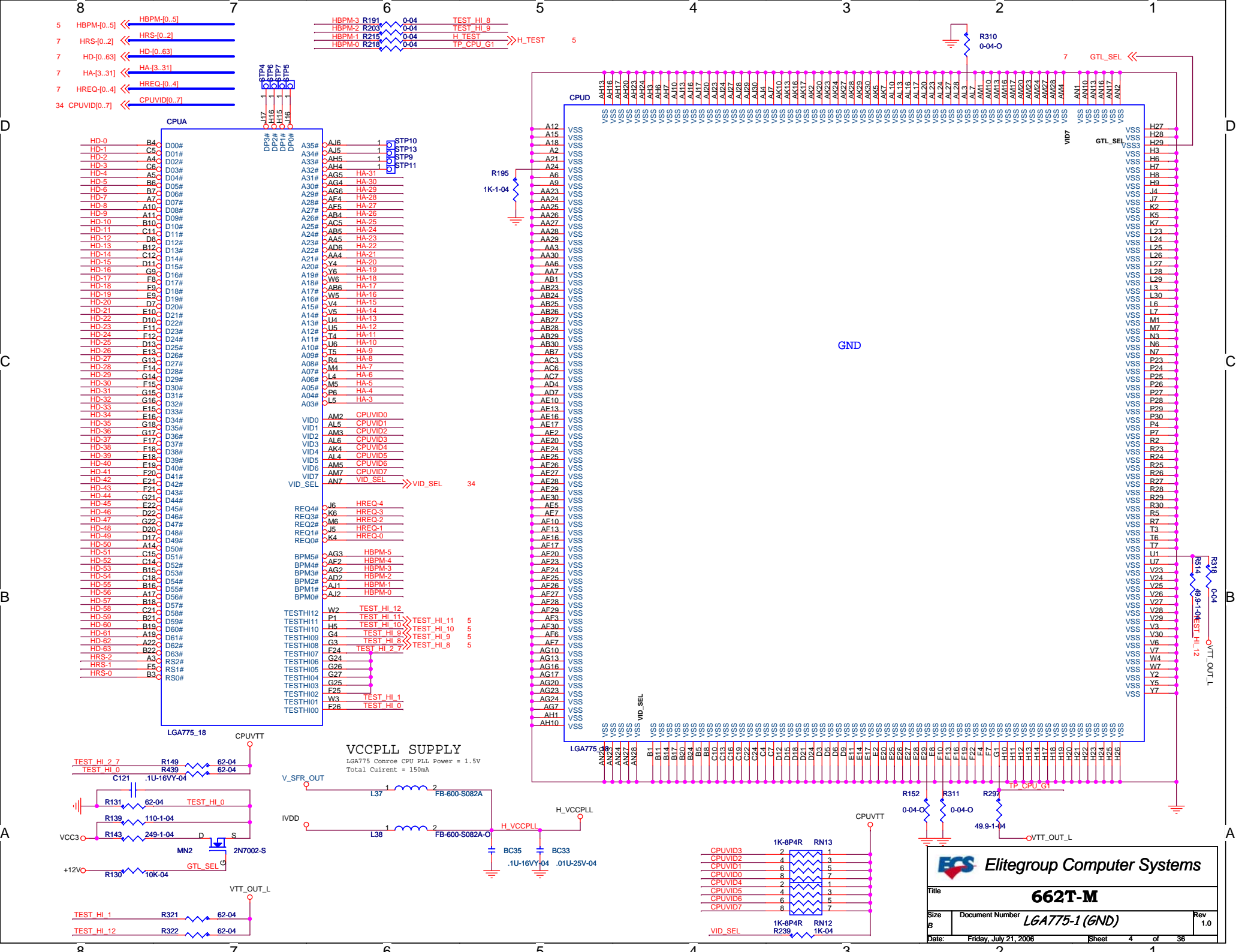
1. Page 5, modified R162 from 100 to 49.9.
2. Page 7, modified R126 from 14 to 10.
. Page 7, modified R117 from 100 to 120.
. Page 7, modified R756 from 619 to 261.
. Page 7, modified SR1 from 100 to 49.9.
. Page 7, modified SR4 from 169 to 100.
3. Page 15, modified R840, R841, and R842 from 1K to 4.7K.
and R843, R844, and R845 from 4.7K to 1K.
4. Page7, modified R804 from 124 to 150.
5. Page7, modified R805 from 500 to 680.
6. Page 34, modified PWM.
7. Page 8, R810 pull high to Vcc3.
8. Page 12, delete 965 KB/MS controller.
. Page 12, modified R873, R874 from 1K to 4.7K.
9. Page 15, modified R73 from 22 to 33.
10. Page 15, modified C68 from 10p to 22p.
. Page 15, modified C101 from 10p to 22p.
11. Page 21, add U26-U29 four ESD IC.
. Page 21, add C1014 and C1016 for EMI.
12. Page 24, add D705-D708 four surge IC.
13. Page 26, add D703 and D704 for preventing pop noise.
14. Page 27, add C1018, C1019, and C1020 for EMI.
15. Page 27, add C1012(1U) to solve MIC issue.
16. Page 27, fine tune audio interface resistance and capacitance.
17. Page 28, changed ITE 8705 to ITE 8712.
18. Page 32, modified R288 from 200 to 187.
19. Page 33, use Q7 and Q8 to replace Vcc_Dual circuit.
20. Page 5, modified to support Smithfield.

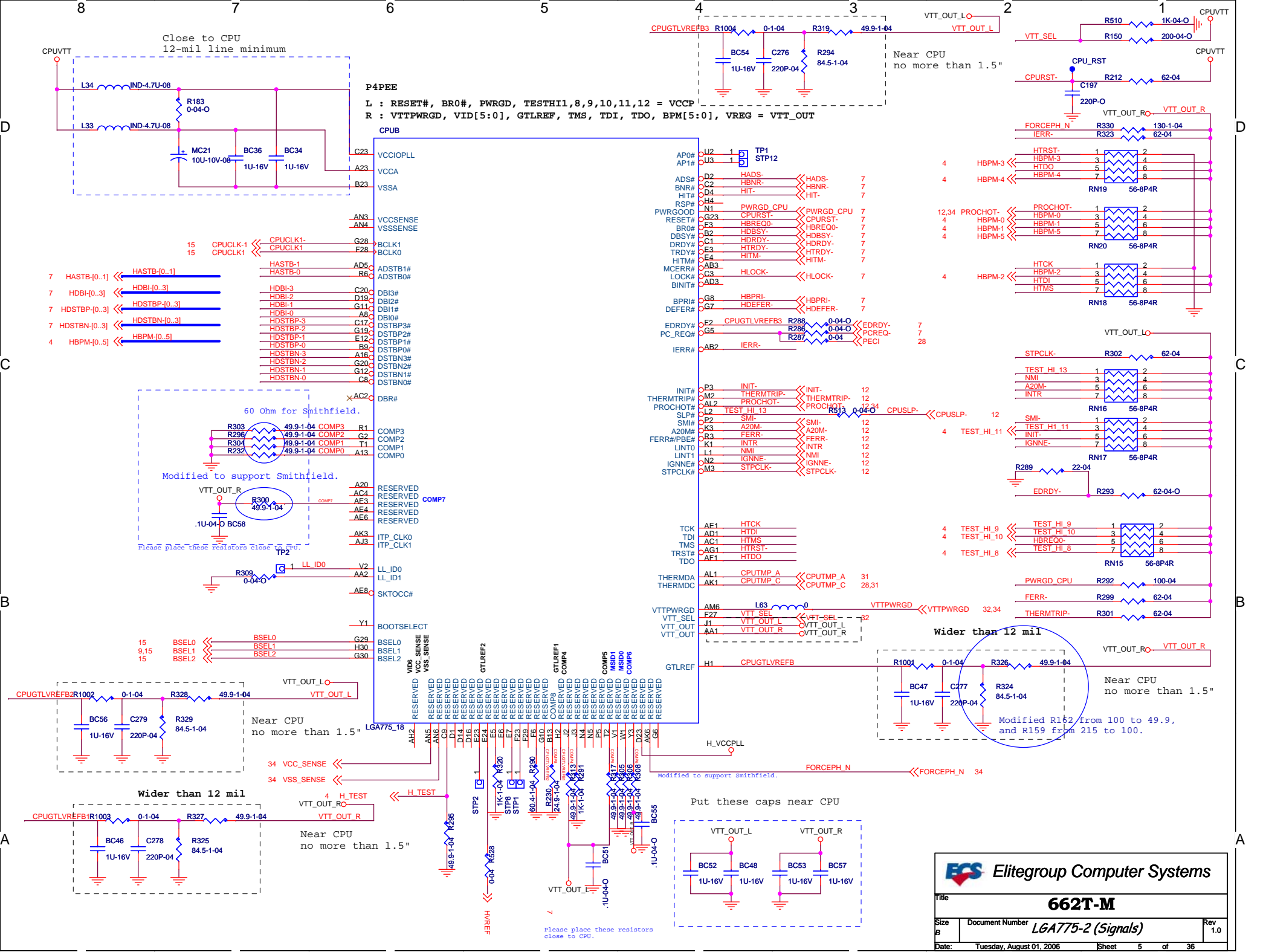
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DESIGNER	Prowind	
LAYOUT	ECS Layout team	
CHECK	Prowind	
APPROVAL		

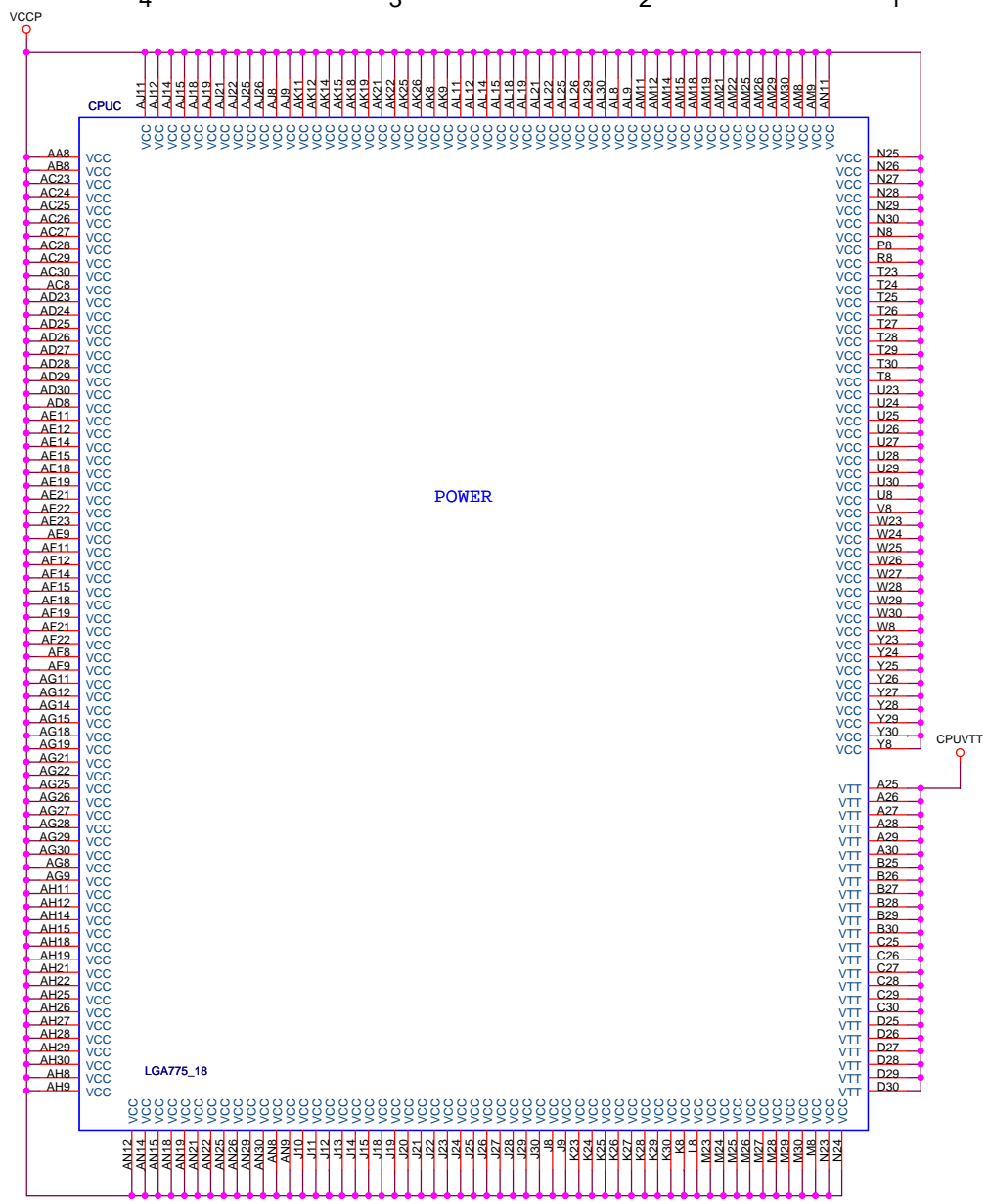
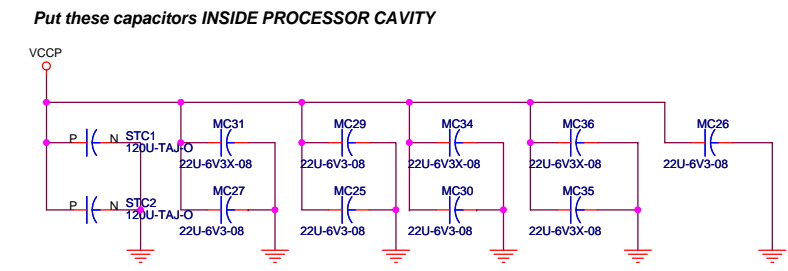
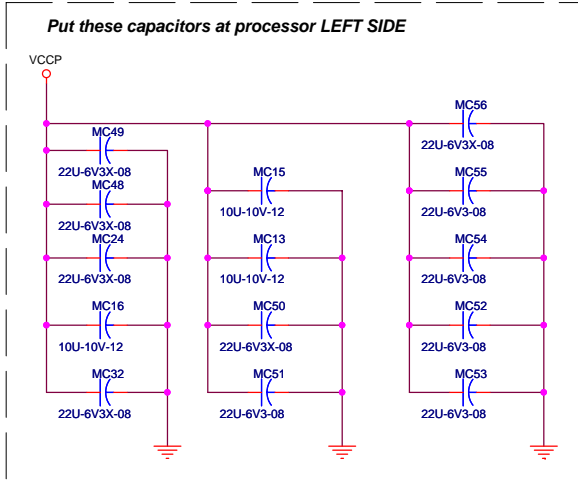
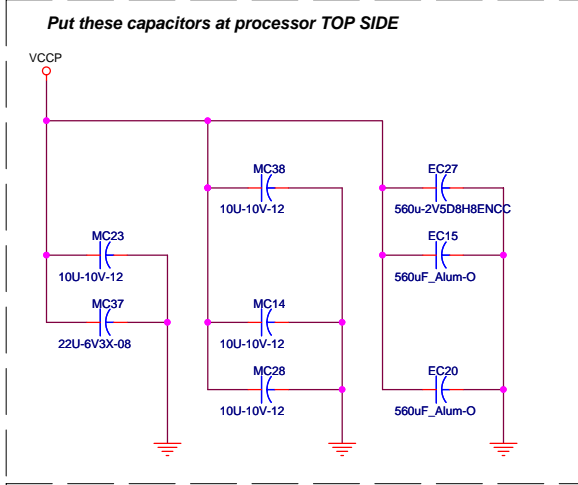
 Elitegroup Computer Systems		
Title 662T-M		
Size Custom	Document Number Cover Sheet	Rev 1.0
Date: Friday, July 21, 2006	Sheet 1	of 36

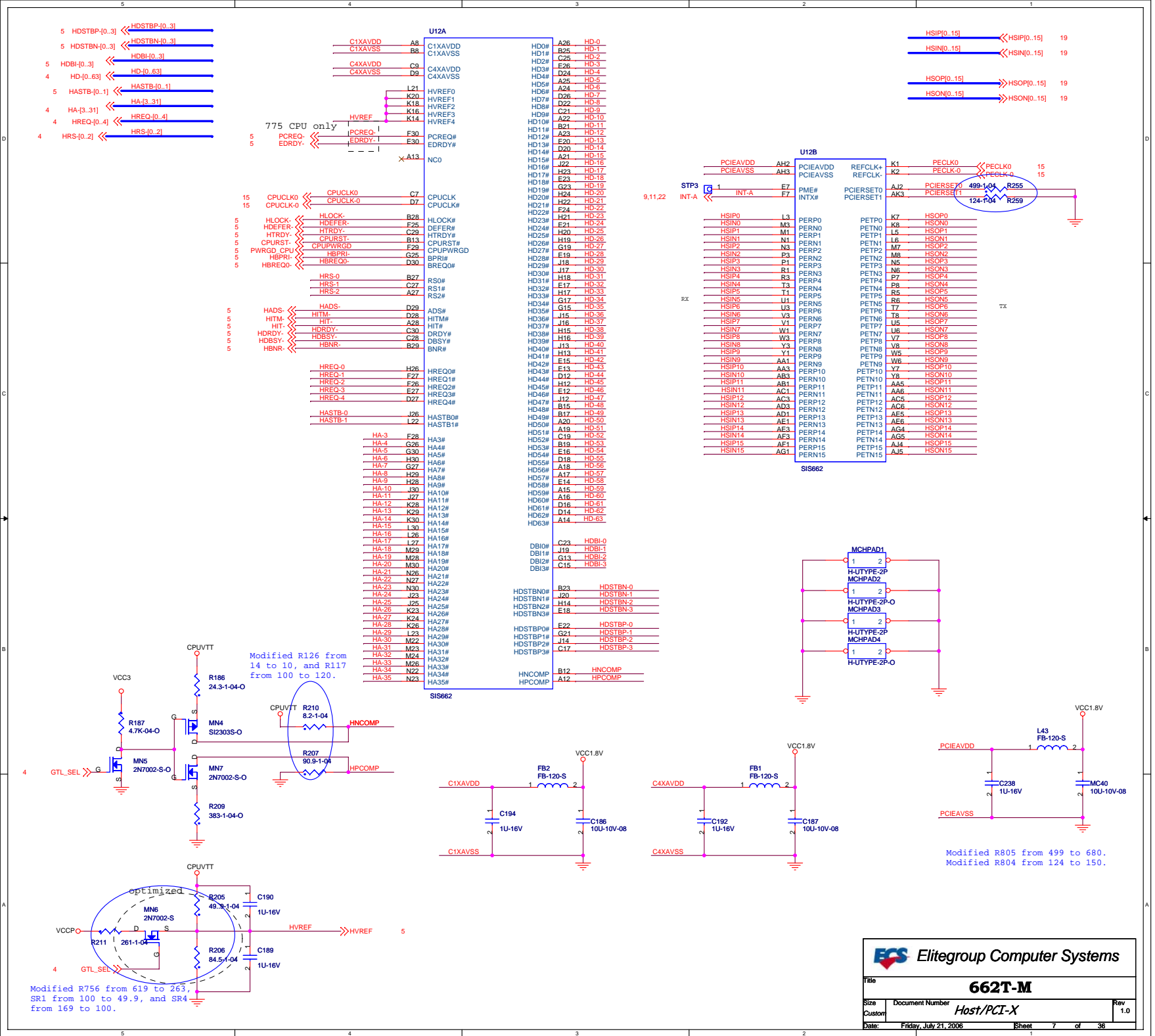


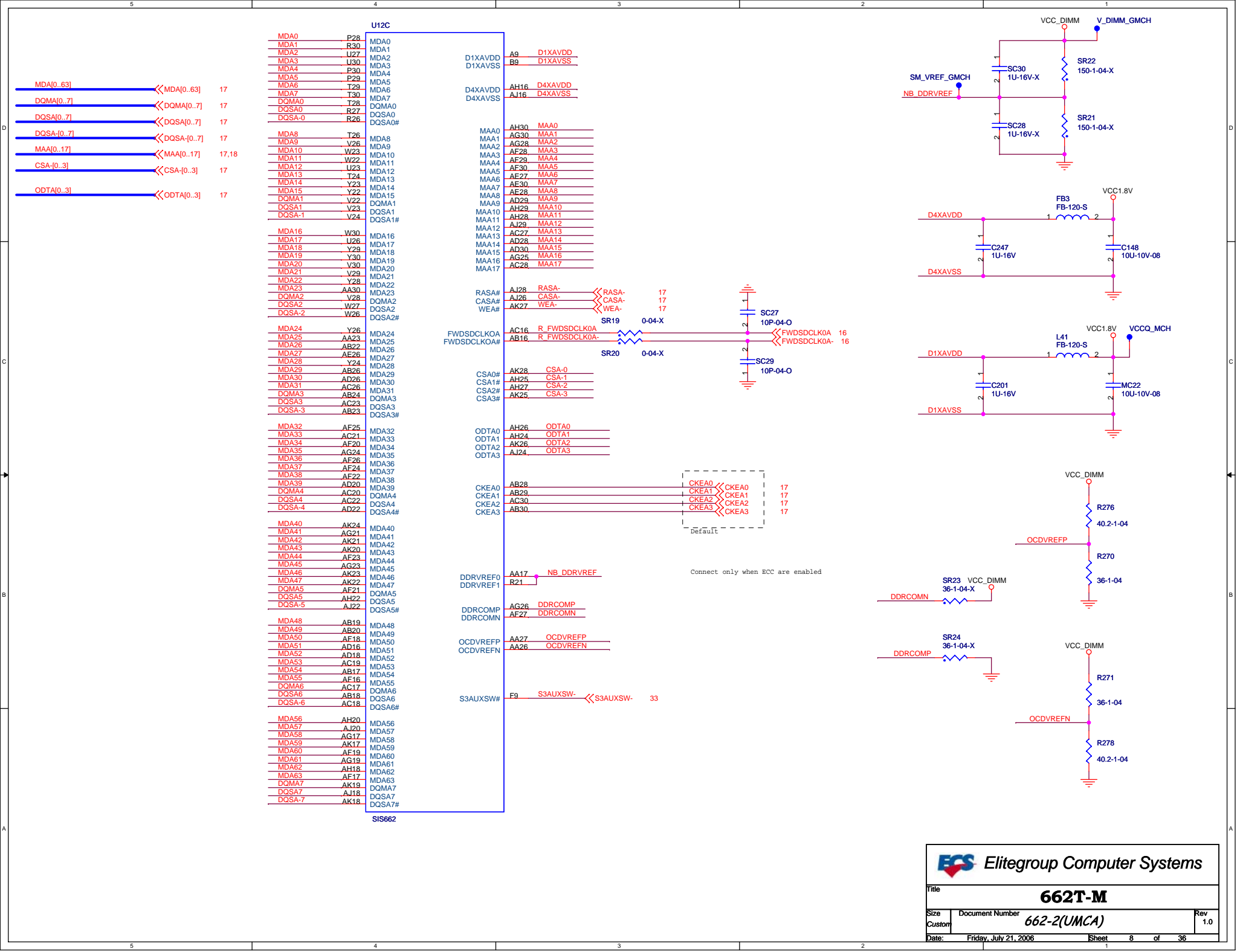


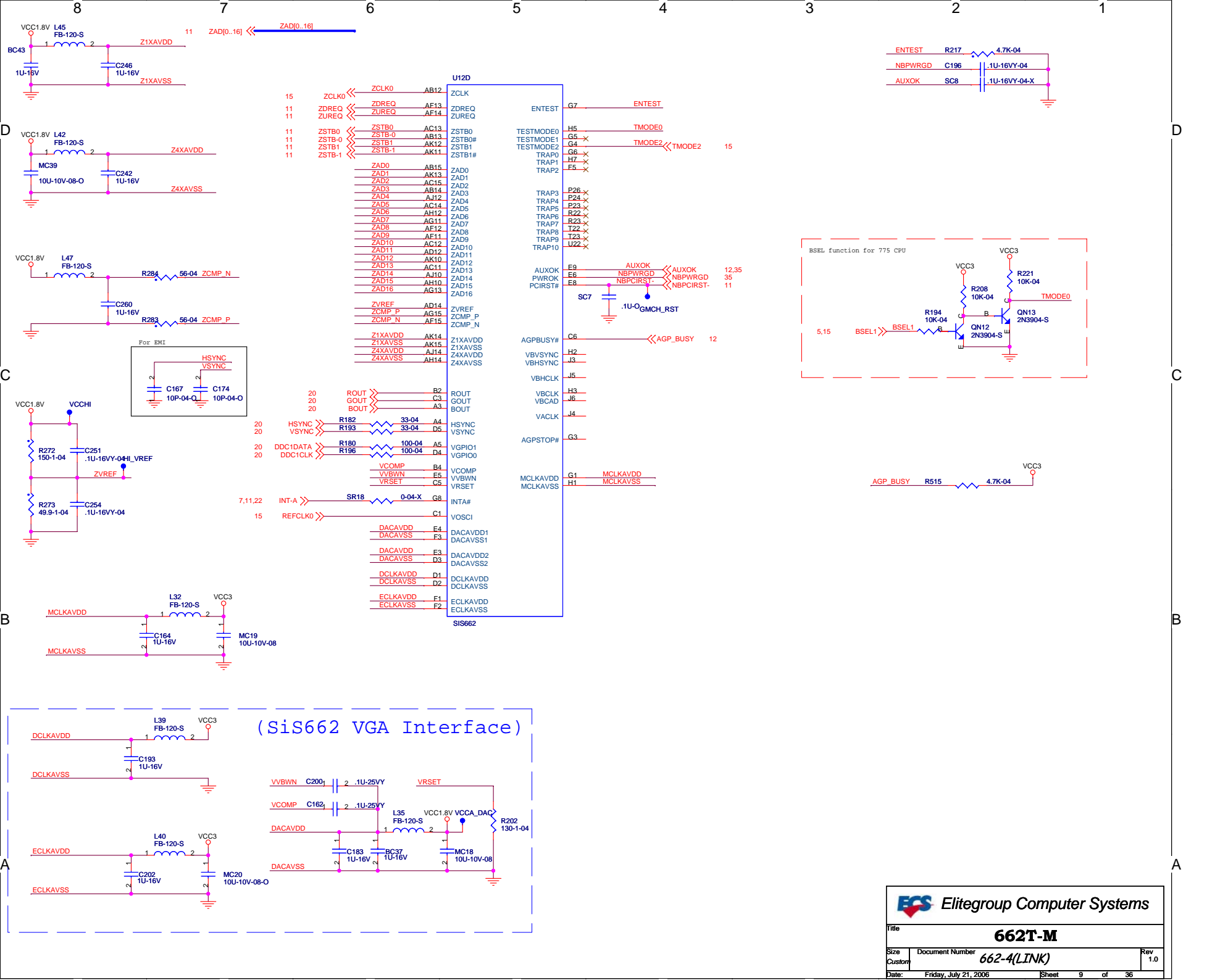


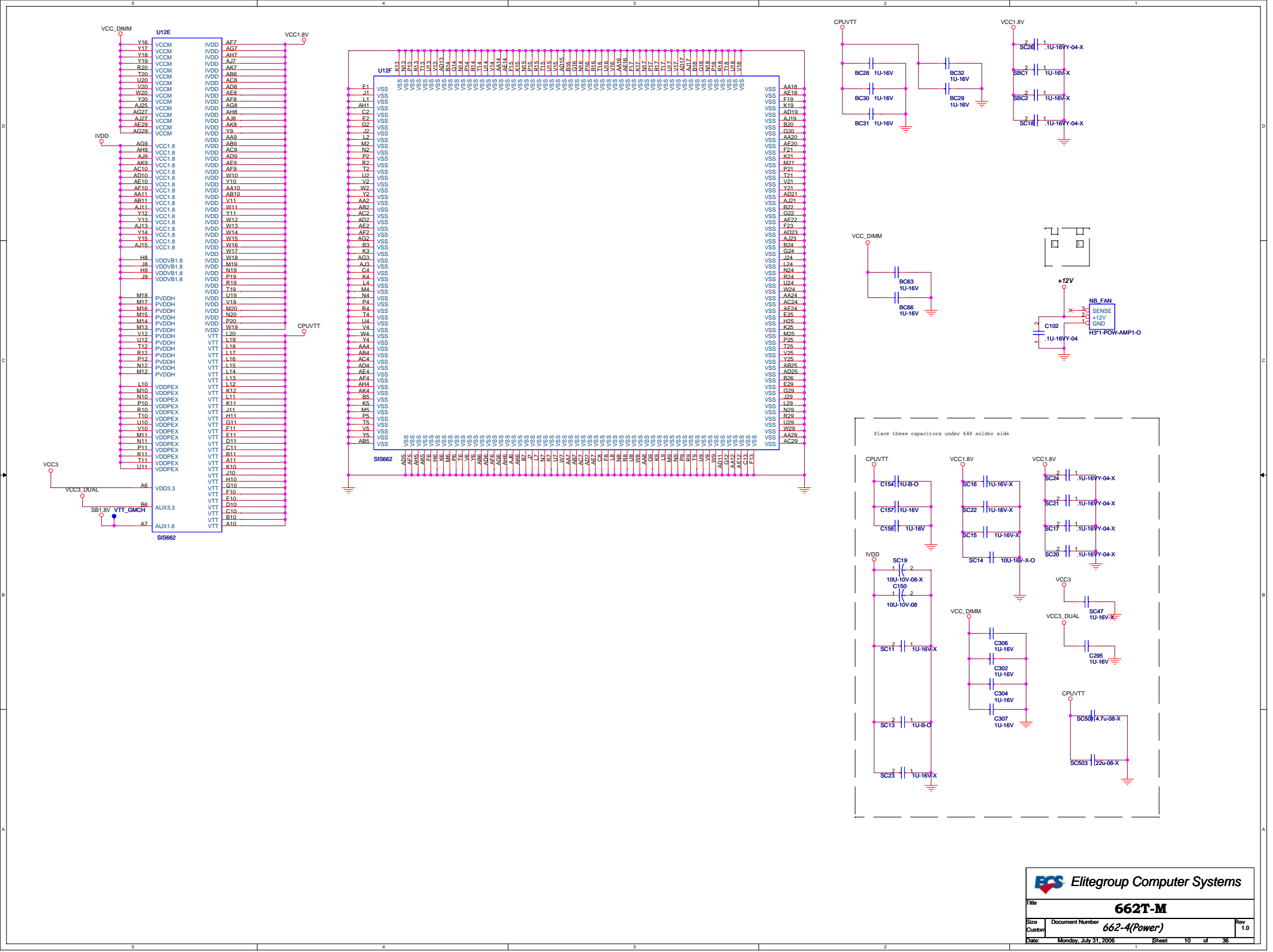


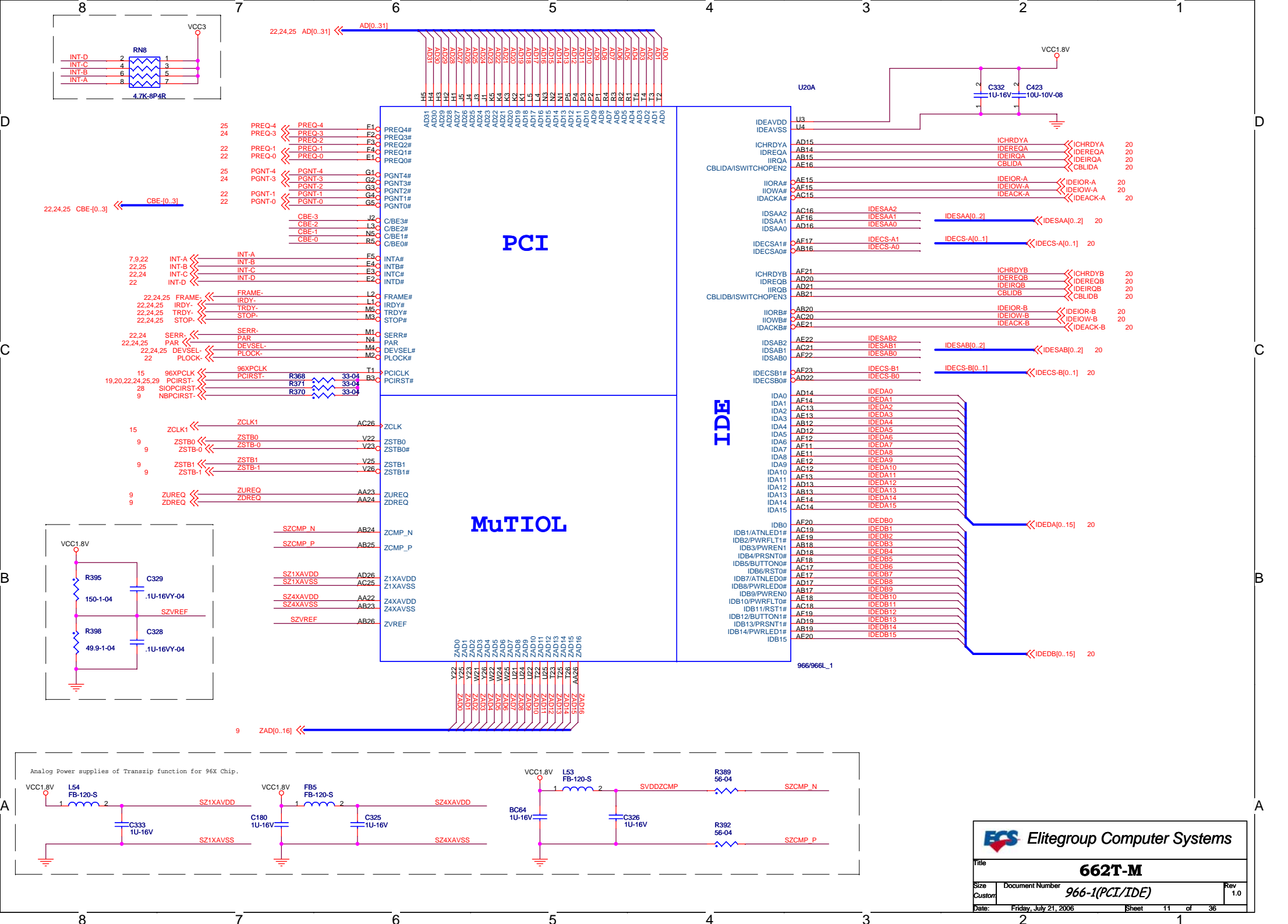


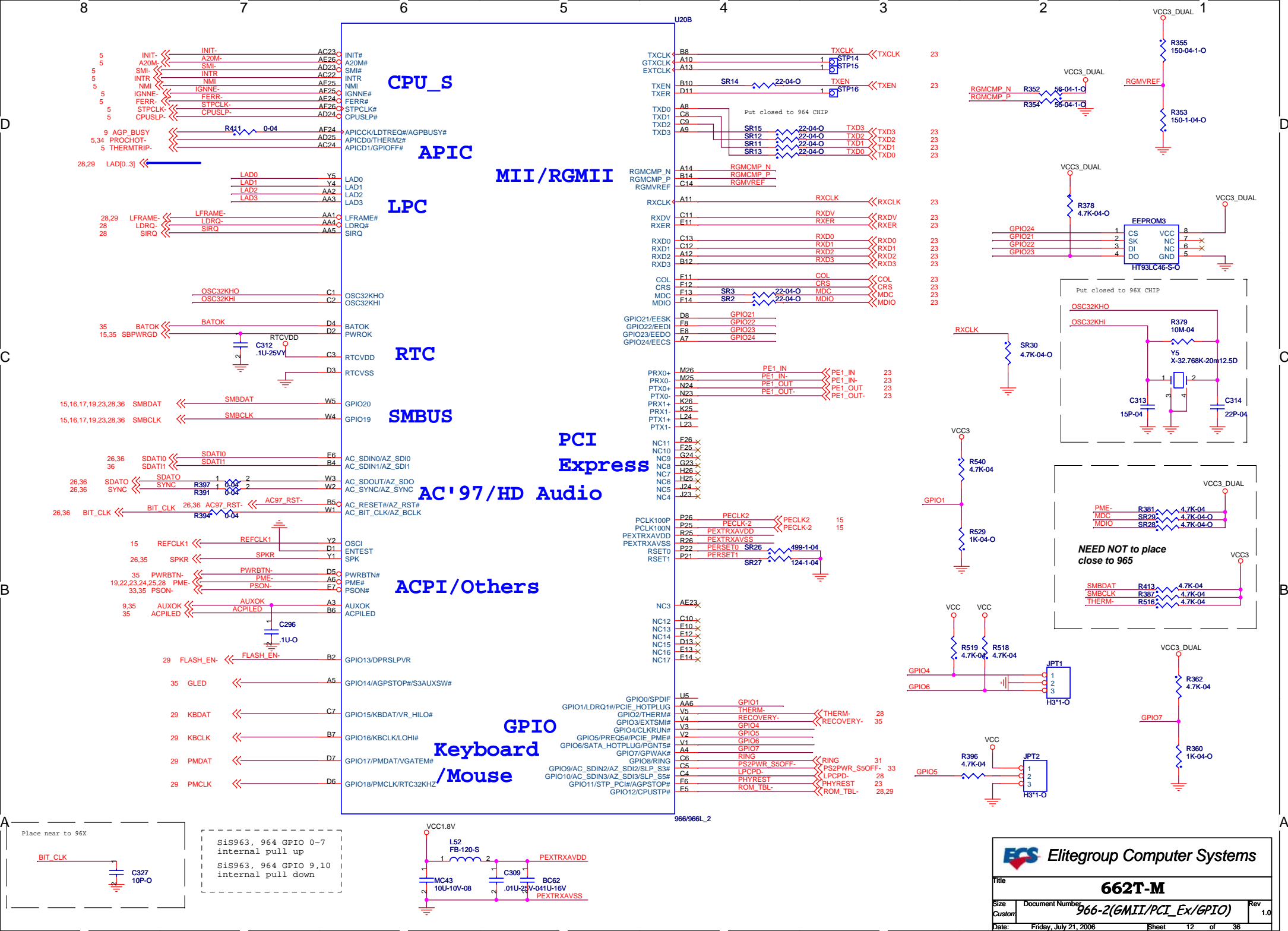


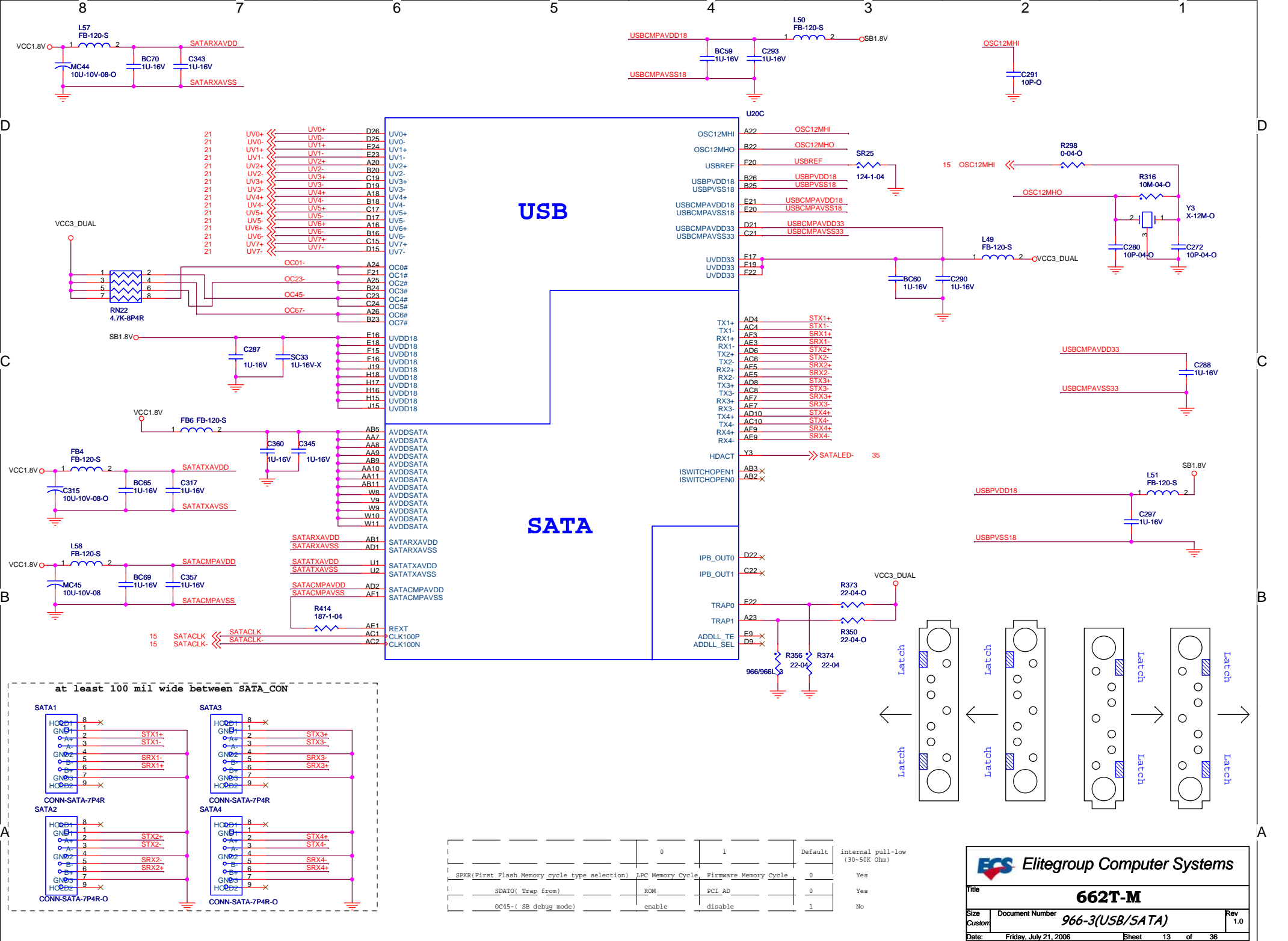


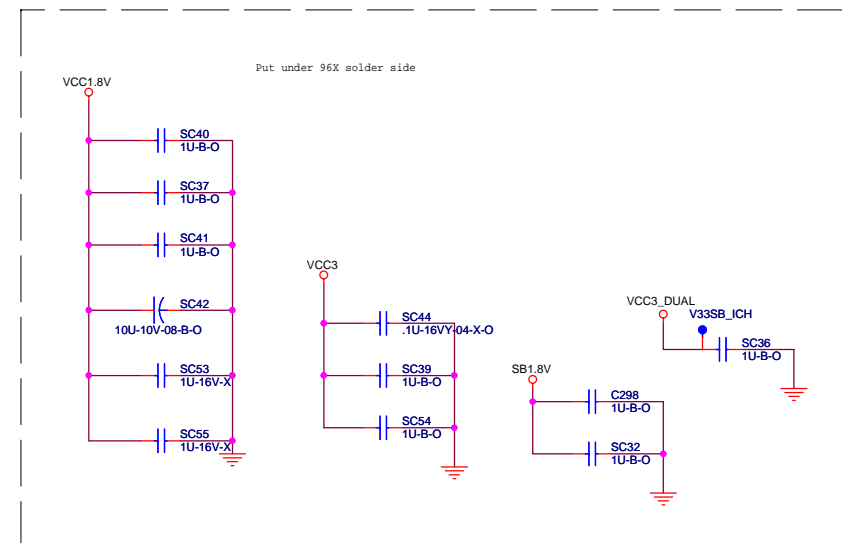
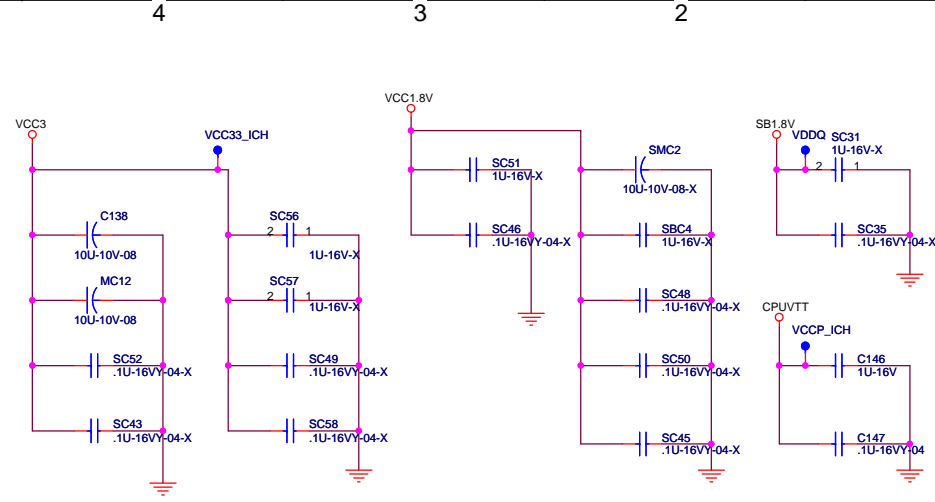
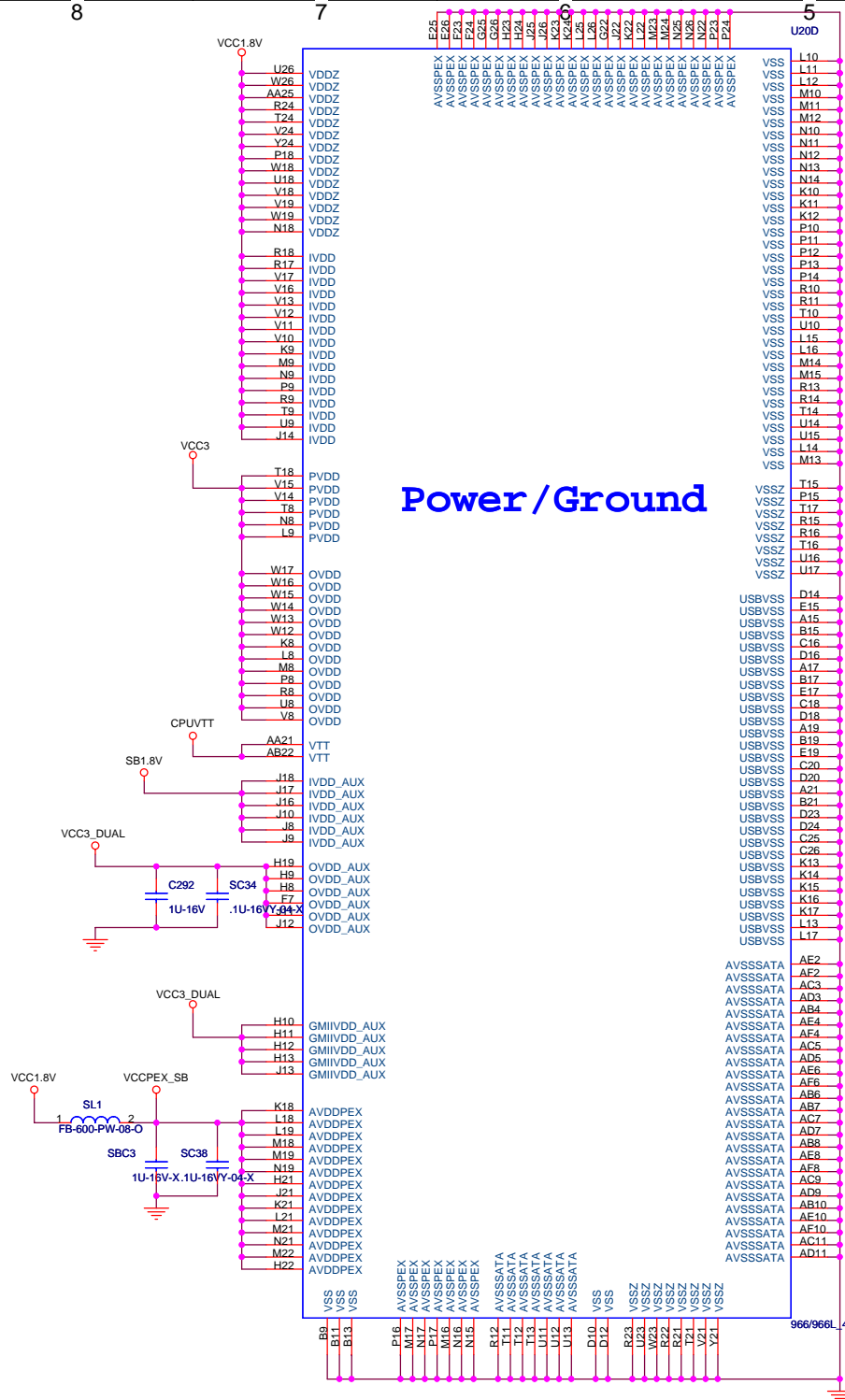


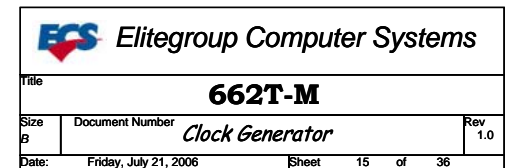
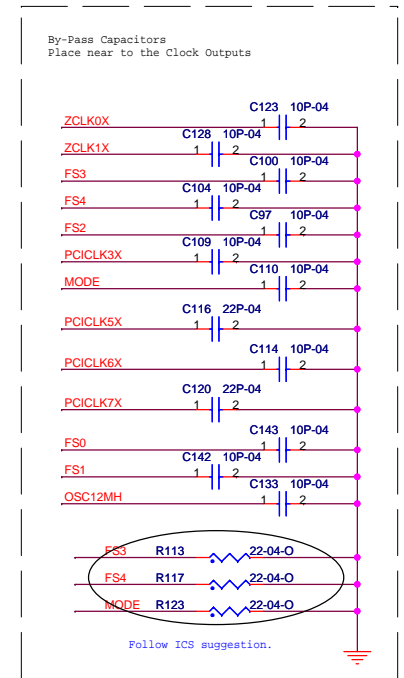








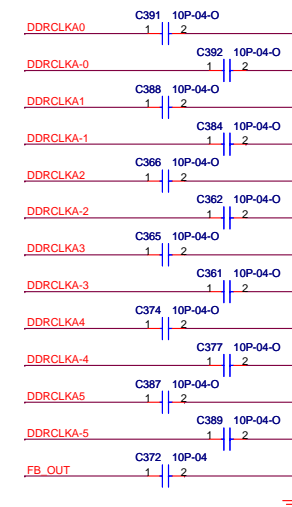
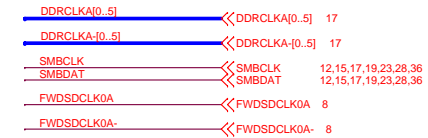
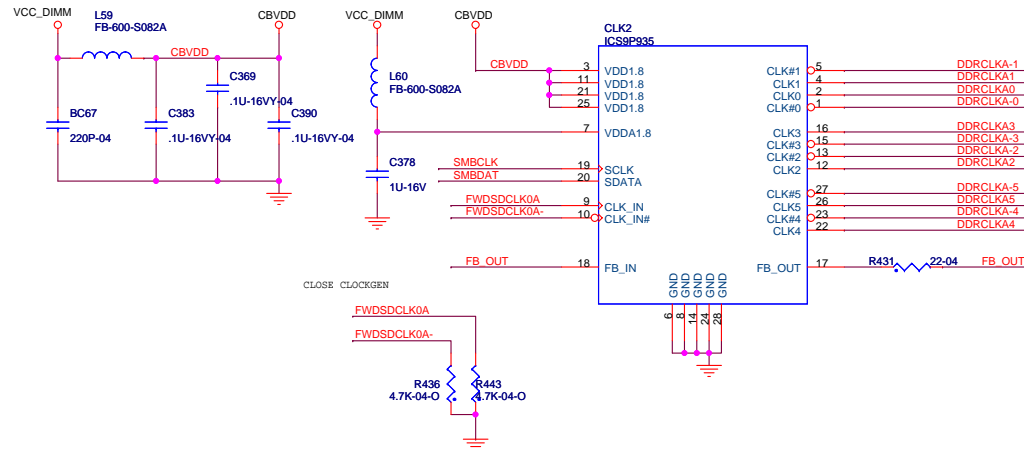


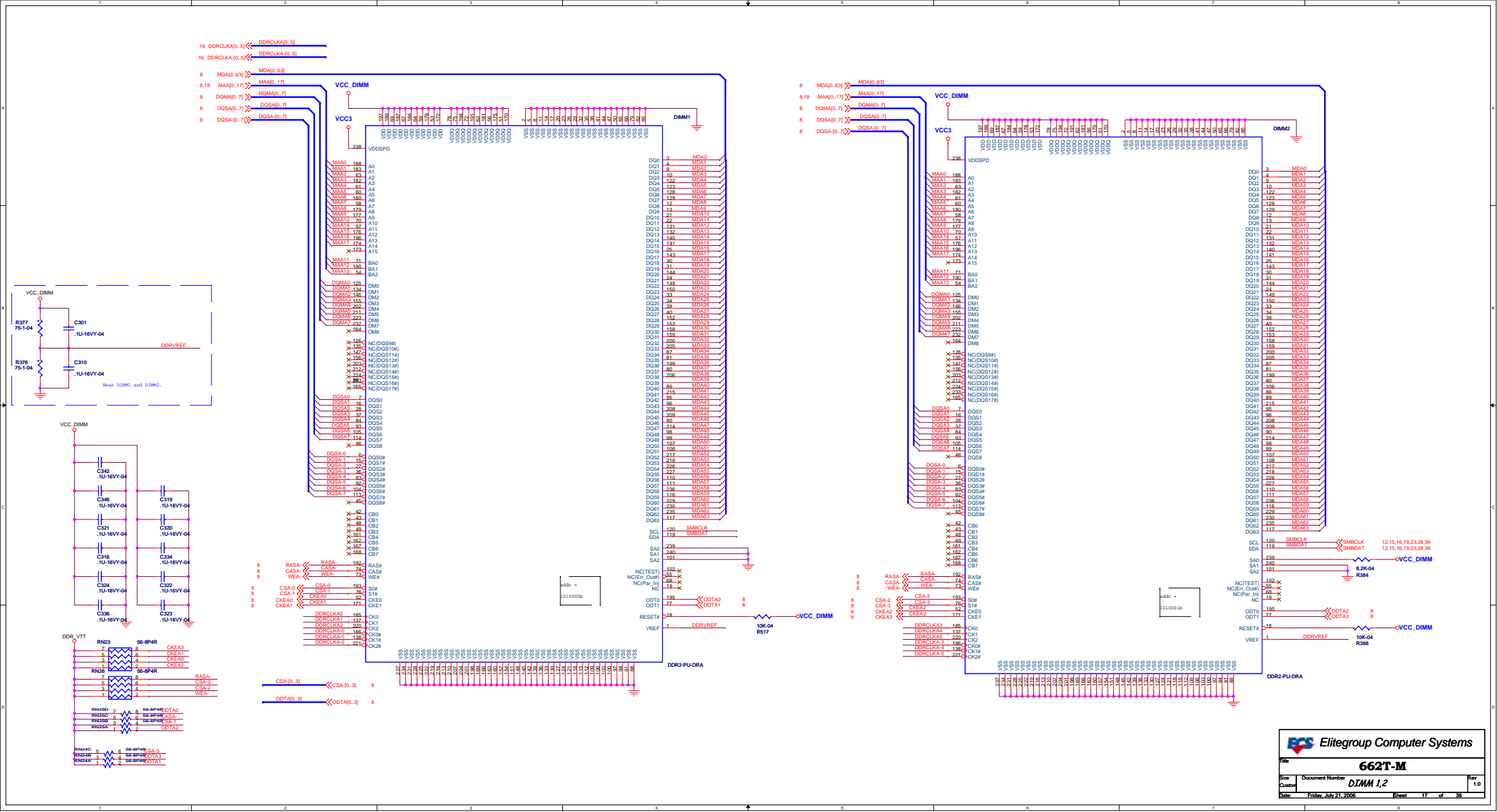


Clock Buffer (DDRII)

(5 OPTIONS)
 1: (ICS) ICS93716
 2: (Winbond)
 3: (ICWorks)
 4: (IMT)
 5: (AMI)

By-Pass Capacitors
 Place near to the Clock Buffer

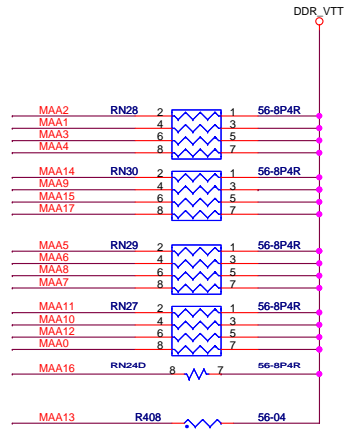




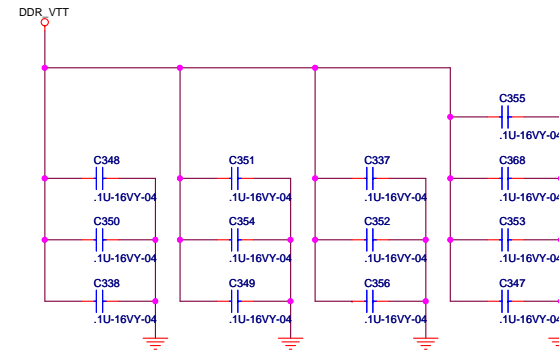
SSTL-2 Termination Resistors

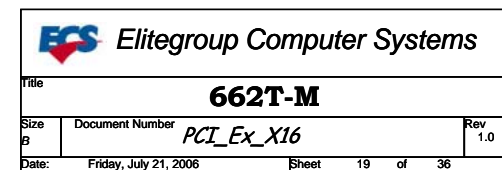
	SDR		DDR		
MD/DQM(/DQS)	LV-CMOS	D/10/-	SSTL-2	1.0	33
MA/Control	LV-CMOS	1.0	SSTL-2	D	33
CS	LV-CMOS	D	SSTL-2	D	47
CKE	D 3.3V		D 2.5V		

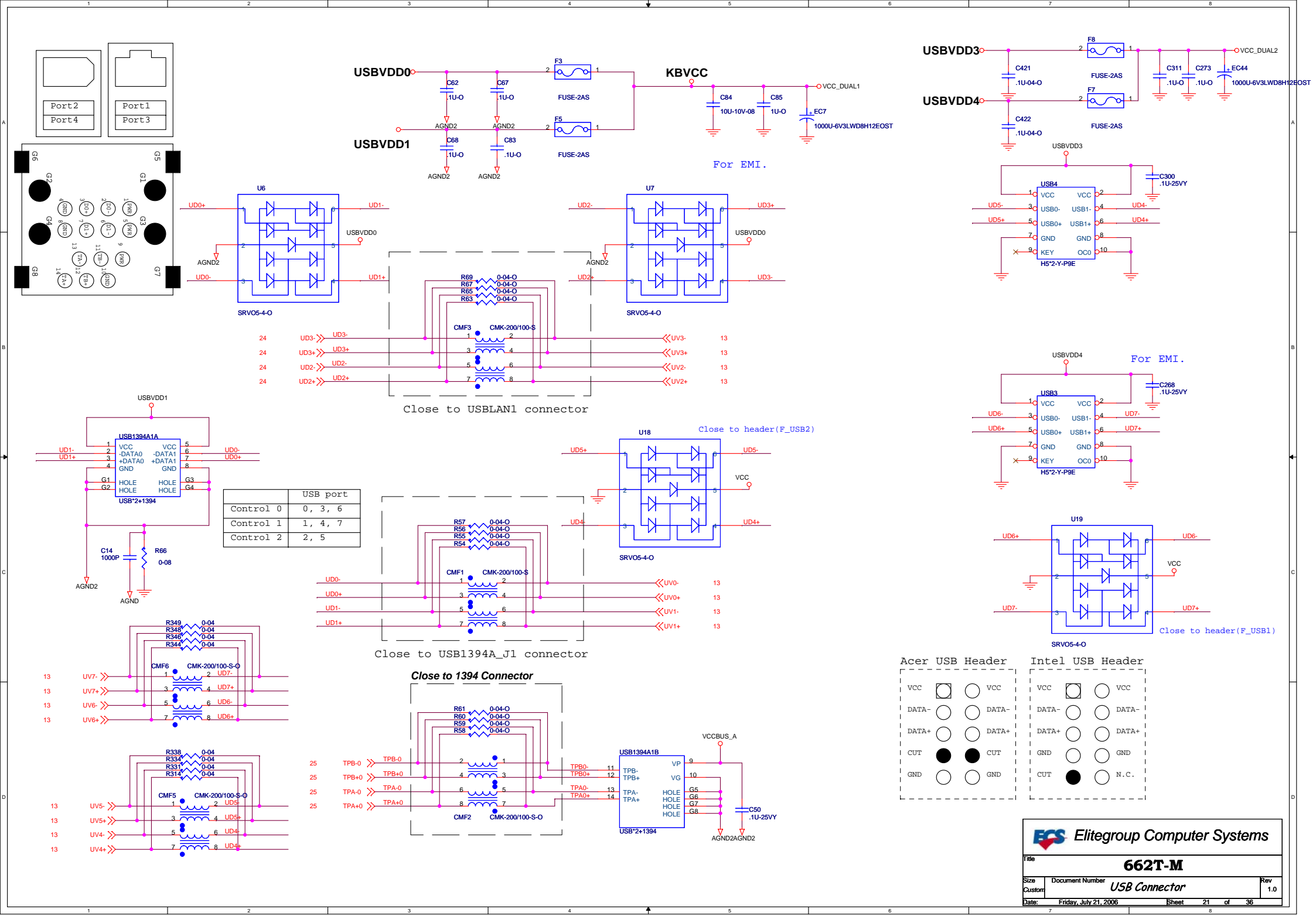
MAA[0..17] << MAA[0..17] 8,17



DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
0603 Package placed within 200mils of VTT Termination R-packs

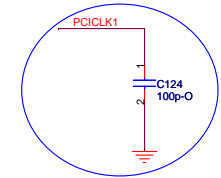
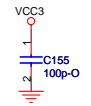
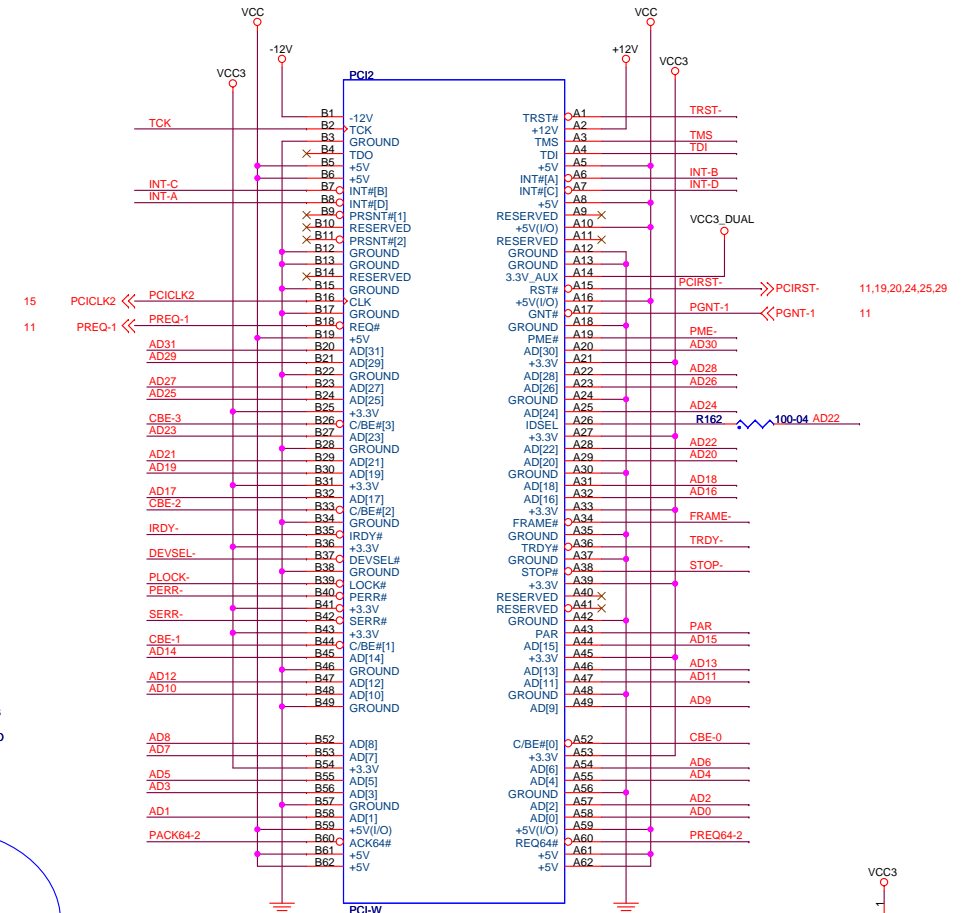
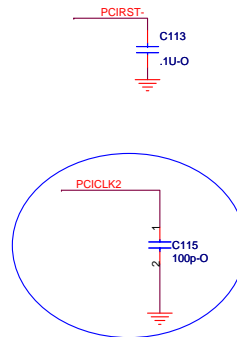
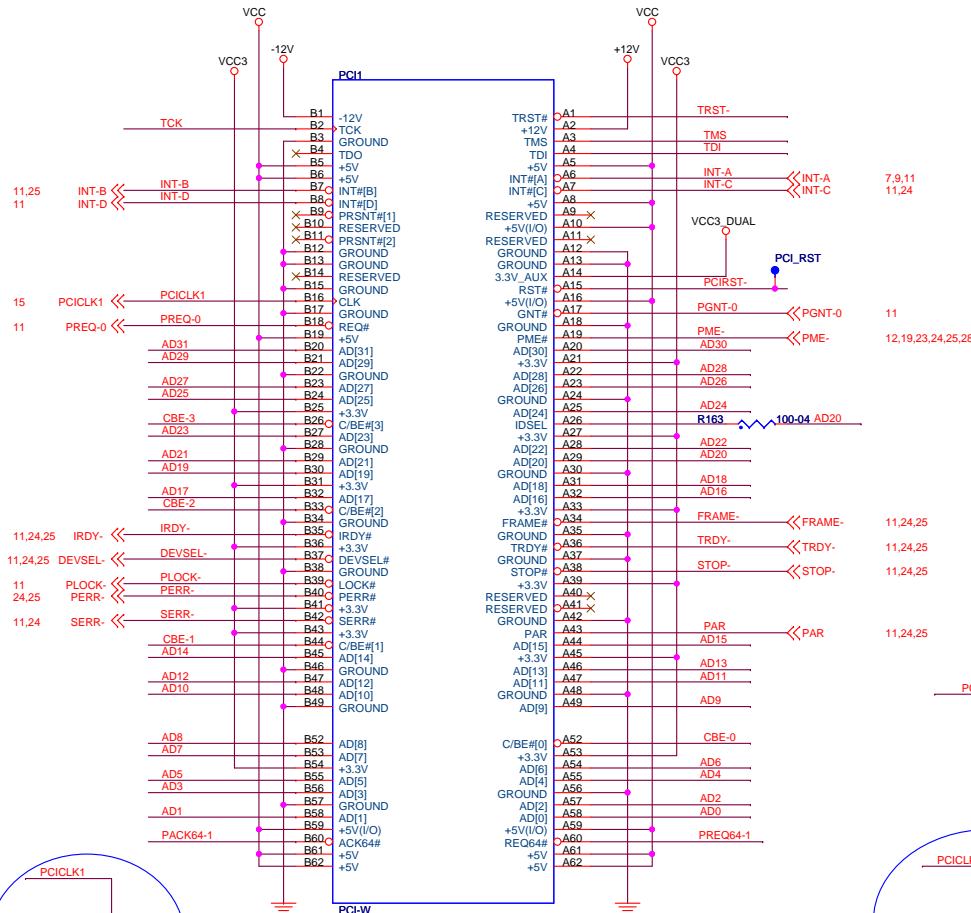






PCI Slot 1 & 2

11,24,25 CBE-[0..3] << CBE-[0..3]
11,24,25 AD[0..31] << AD[0..31]

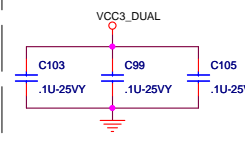
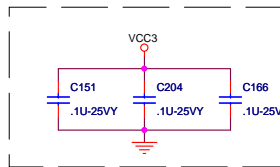
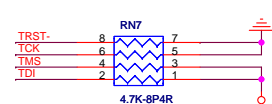
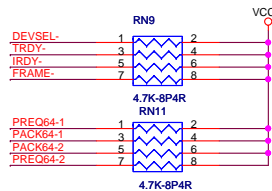


IDSEL=AD20
INT[A,B,C,D]
PCIx3=slot2
PCIEx1+PCIx2=slot1

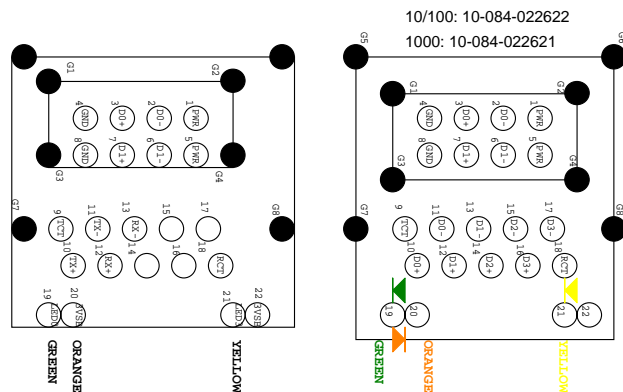
IDSEL=AD22
INT[B,C,D,A]
PCIx3=slot3
PCIEx1+PCIx2=slot2

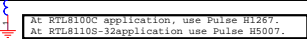
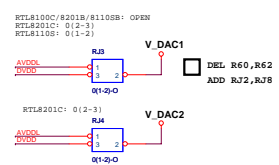
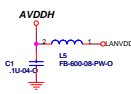
Please place the cap close PCI Slot.

Please place the cap close PCI Slot.

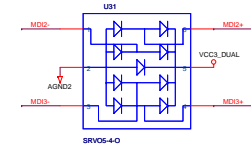


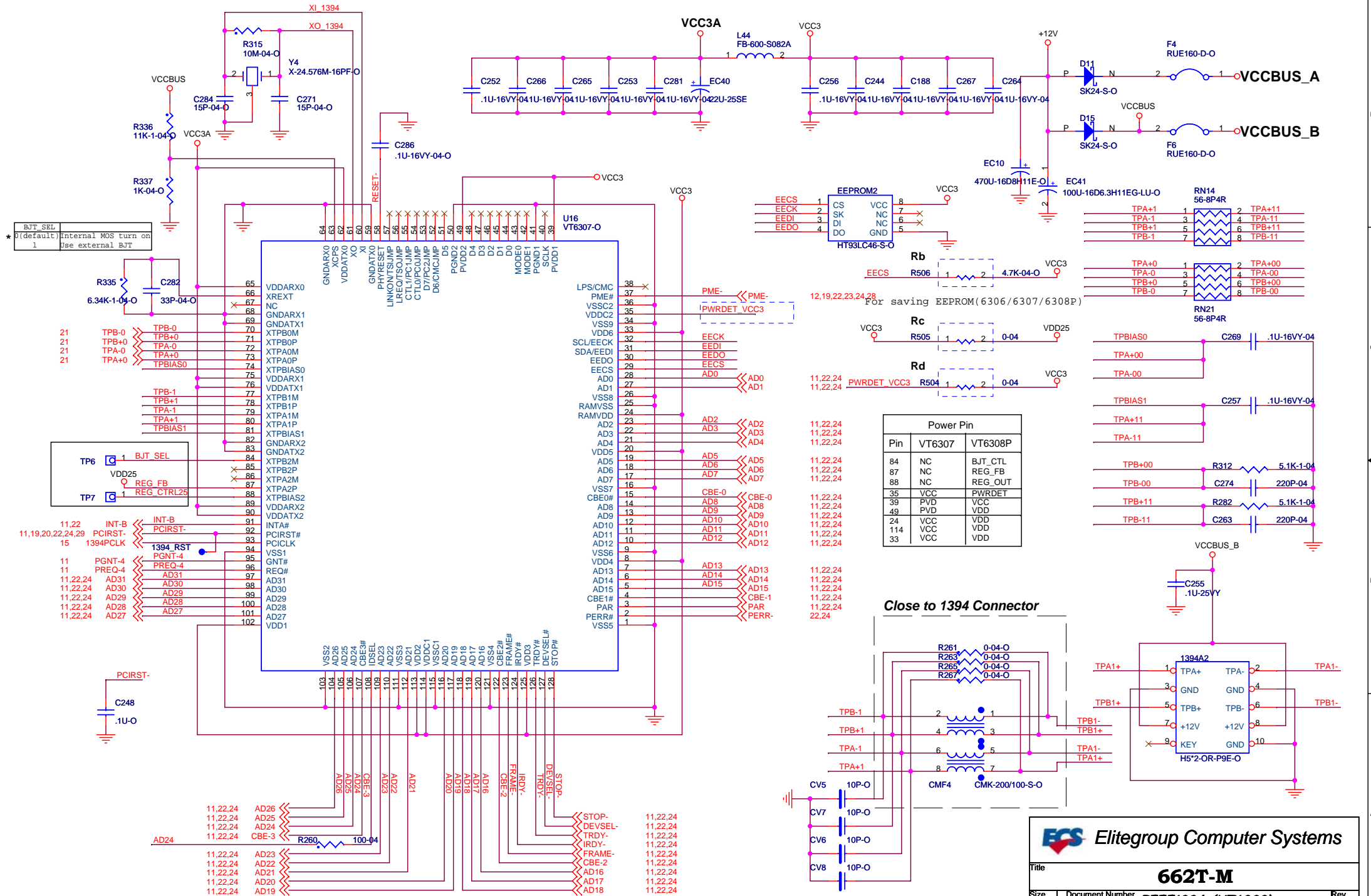
每個 PCI 插槽 pin A33
各放一顆

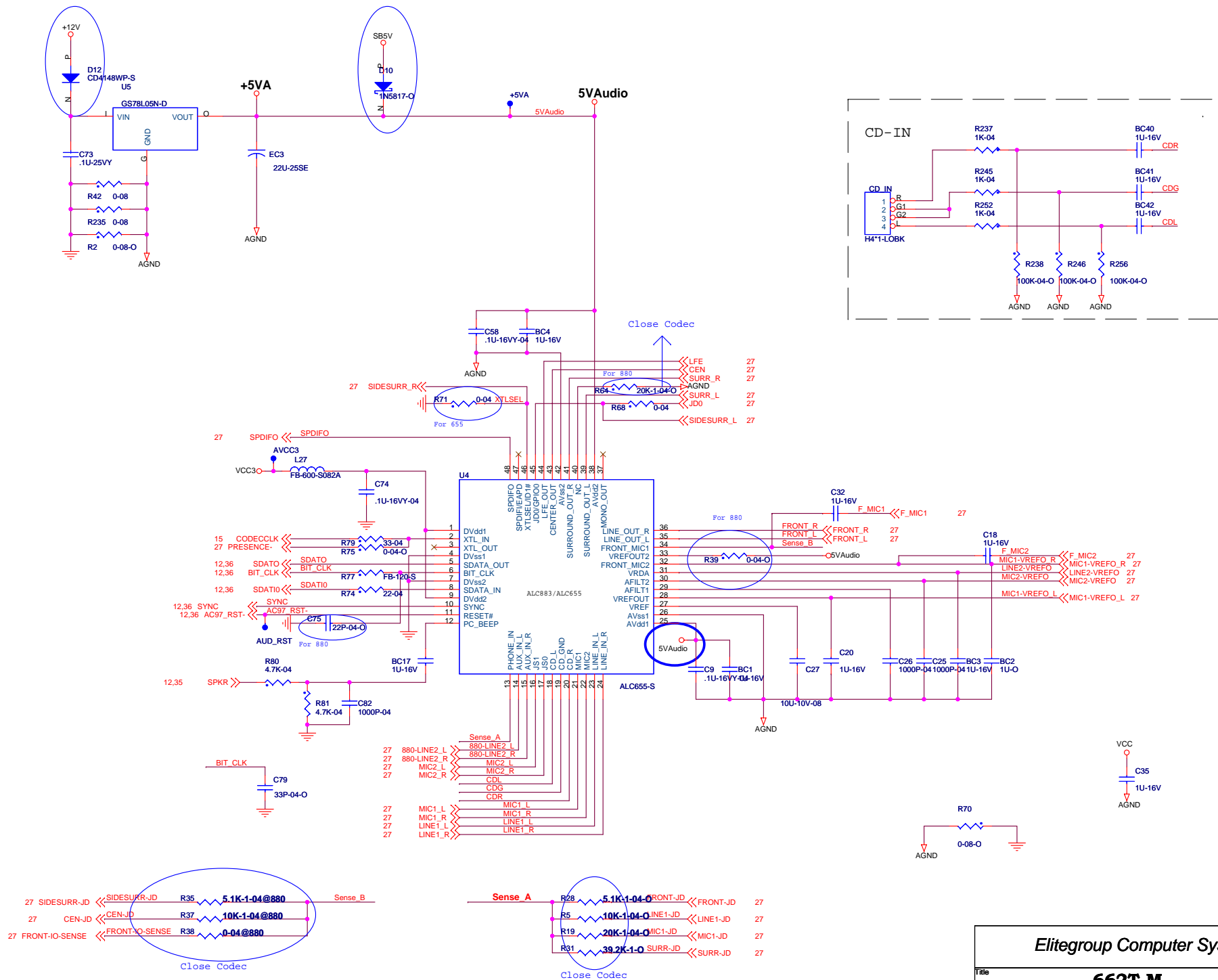


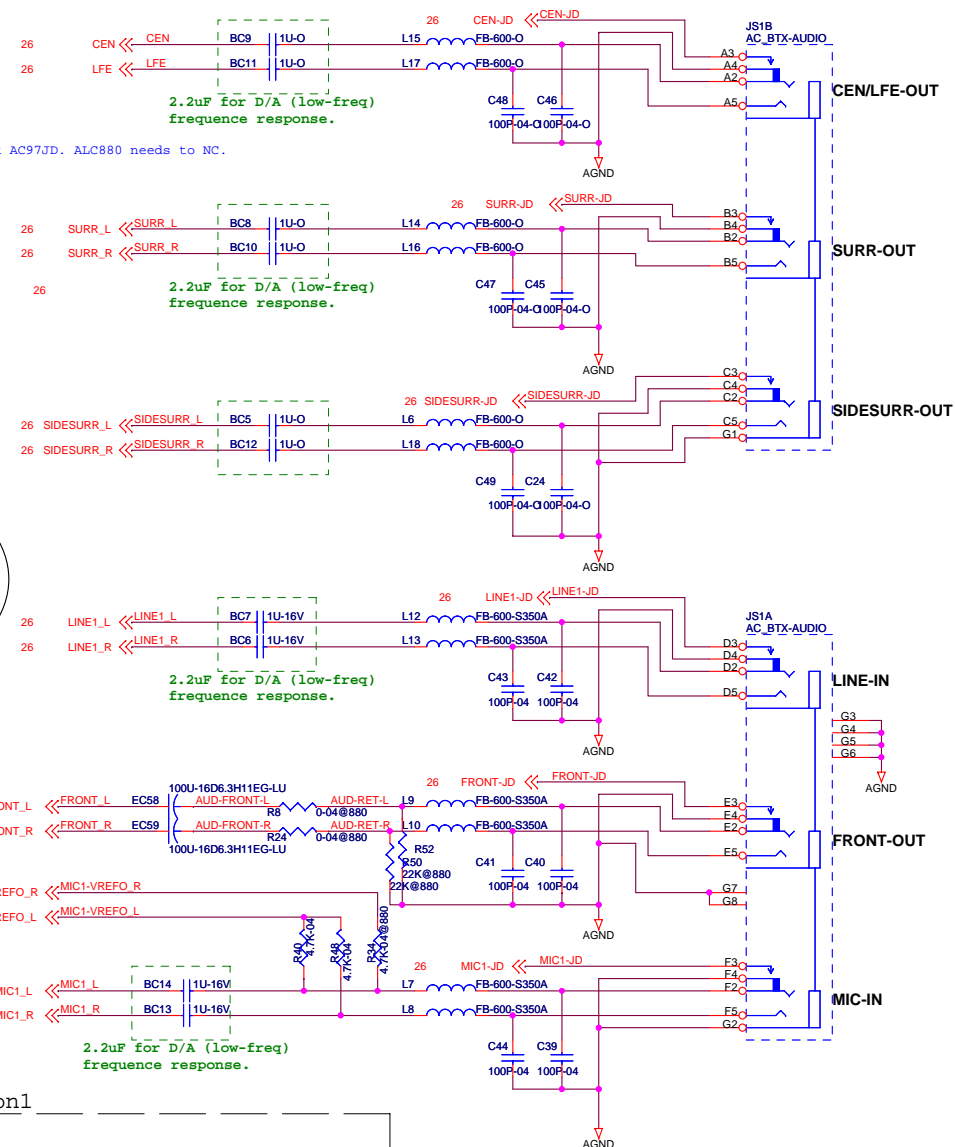
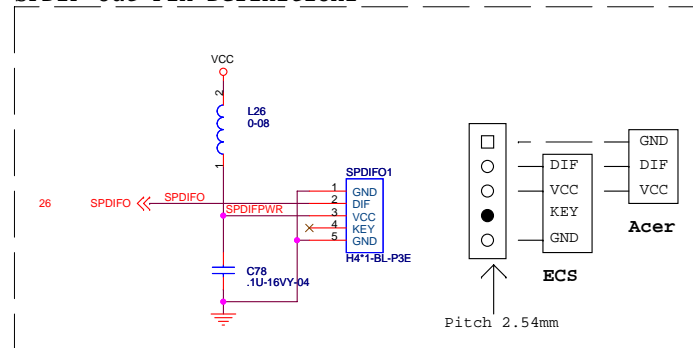
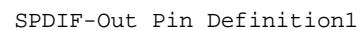
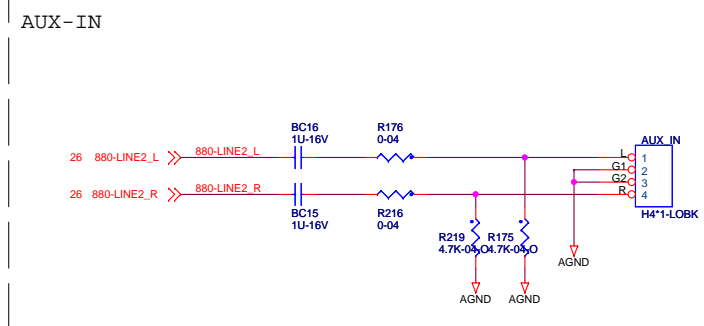
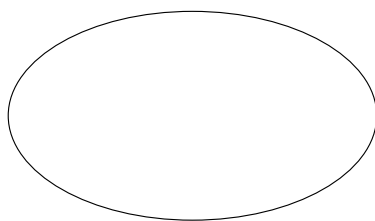
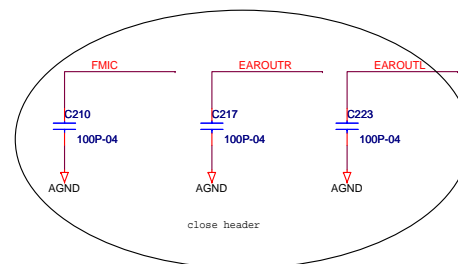
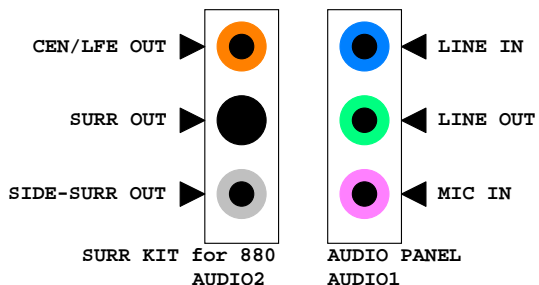


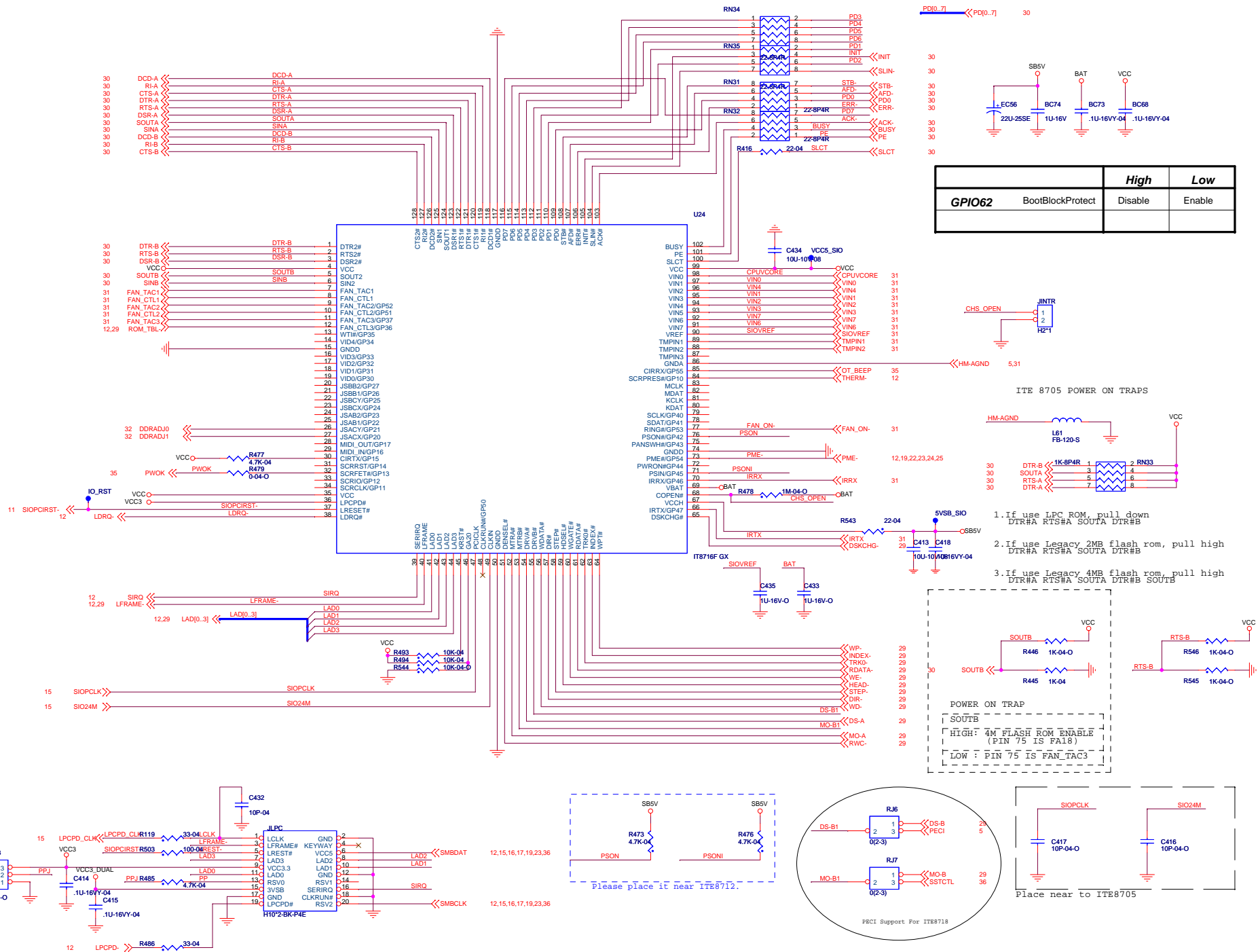
At RTL8100C application,
remove R21, R28, R12, R14,
C18, C10, C52, C53, C54, and
change C51 value from .01uF
to .1uF.

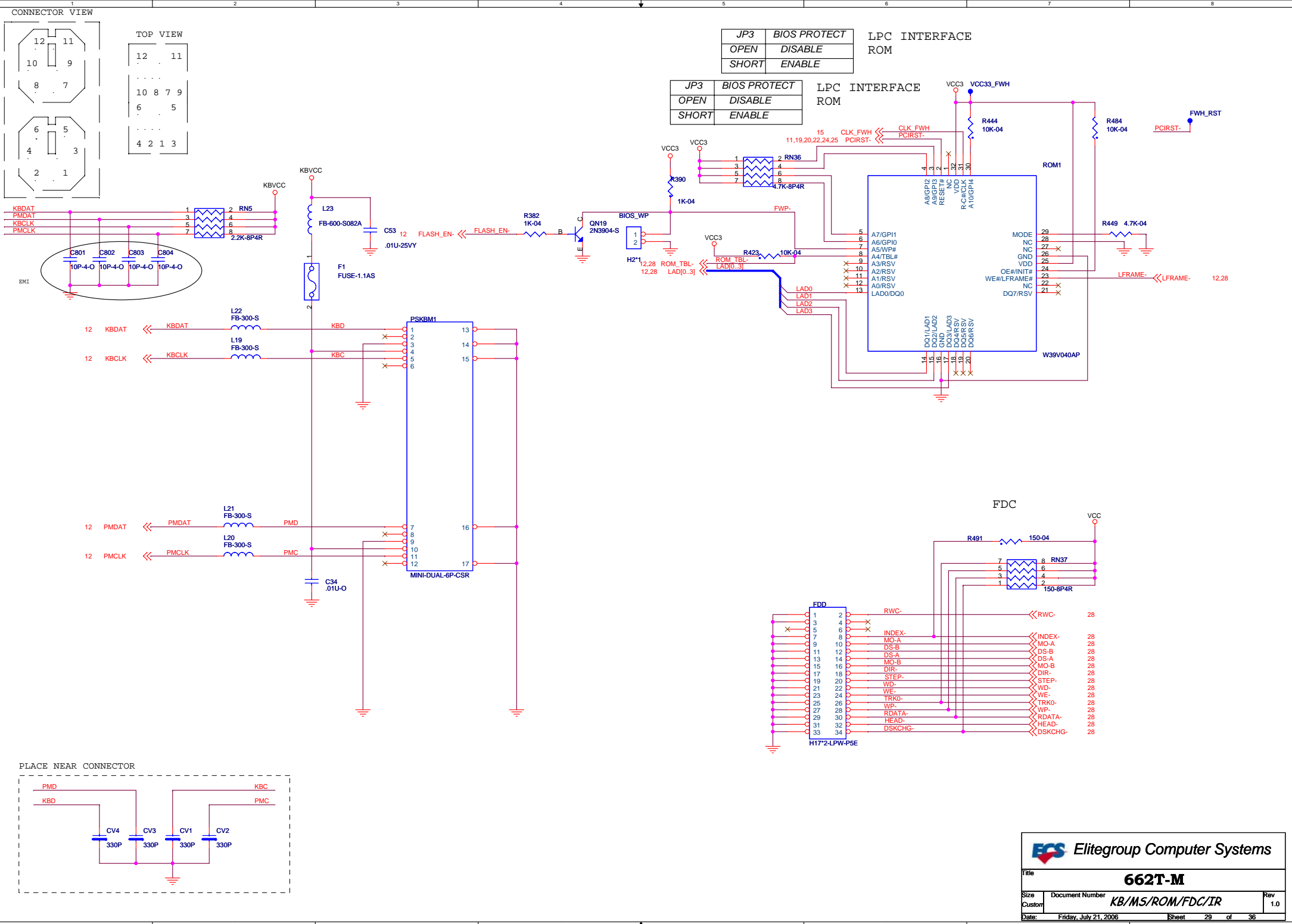






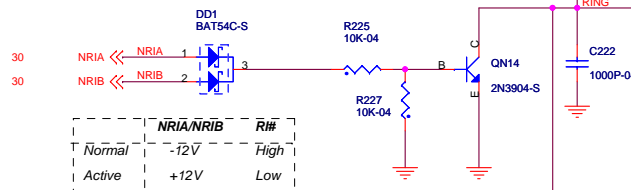




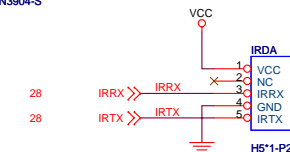
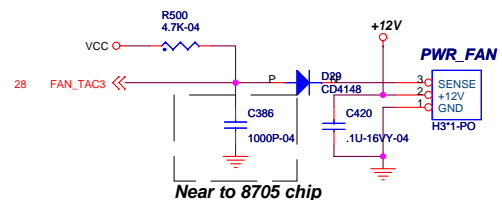
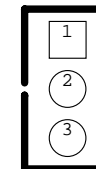
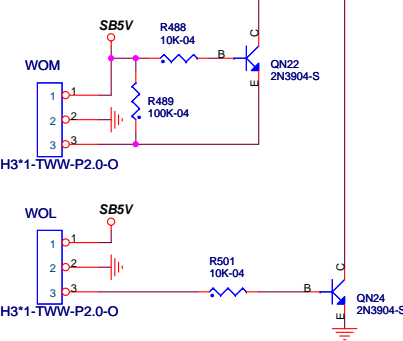


Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA .

□

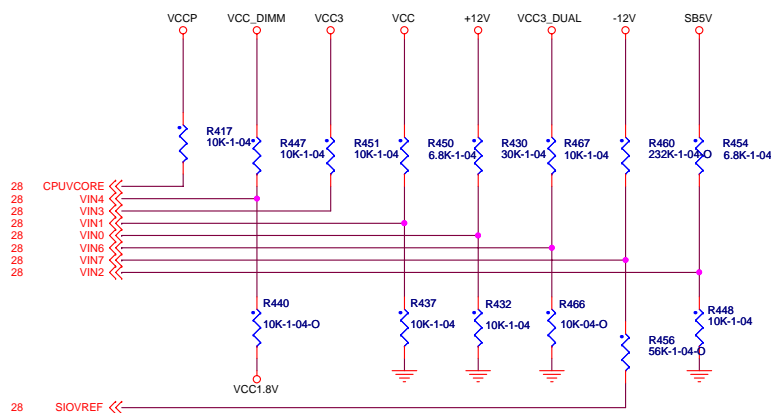
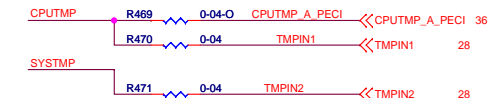
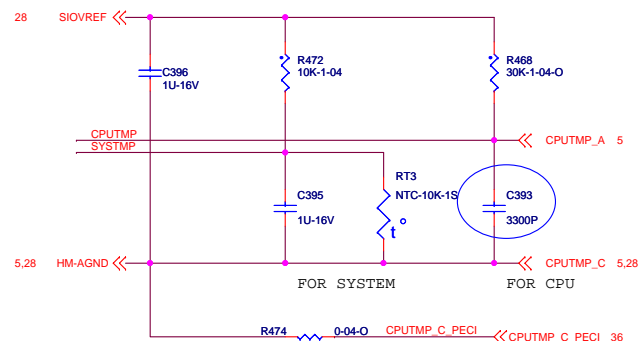


3pin header: R223, EC46, R216, R219,
Q5, R324, QN704, R323



Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode



FOR SYSTEM

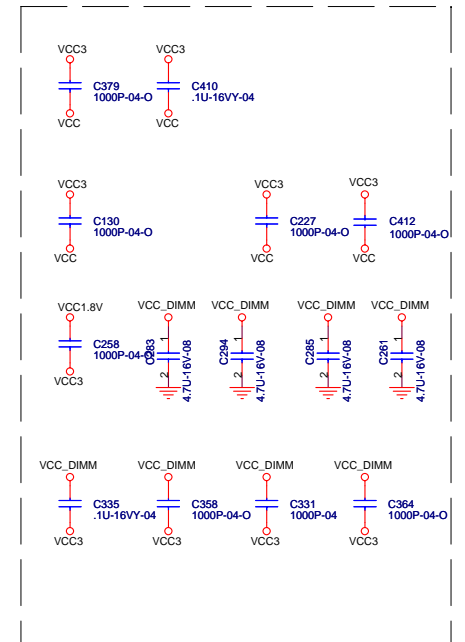
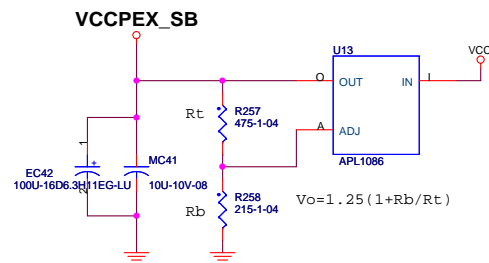
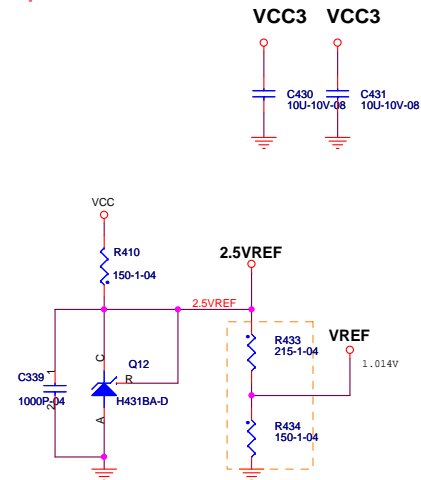
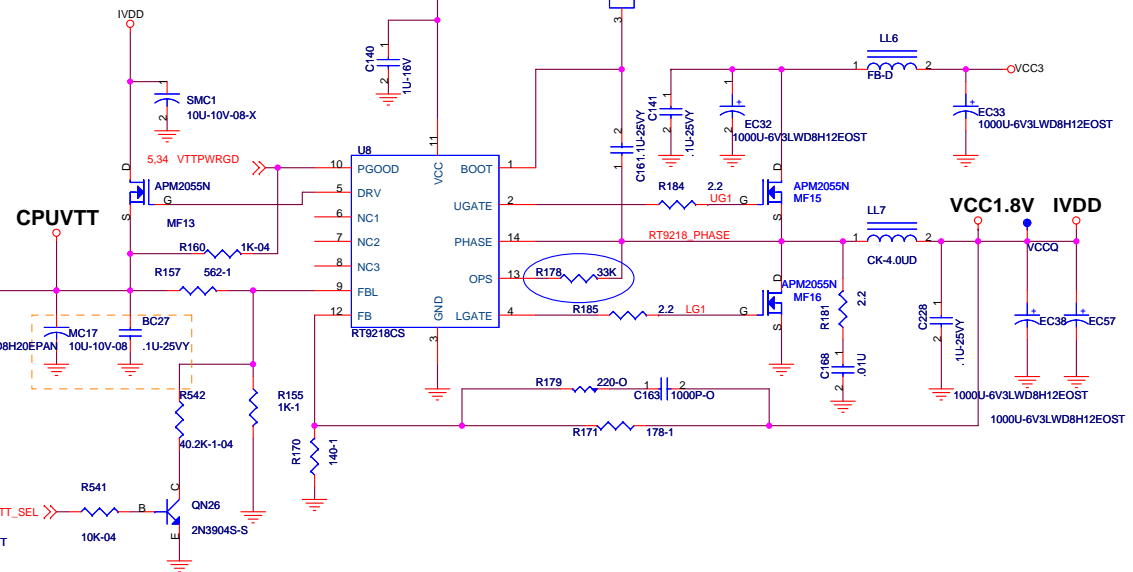
FOR CPU



Elitegroup Computer Systems

Title				662T-M			
Size	Document Number						Rev
Custom	<i>HM / FAN / RING</i>						1.0
Date:	Tuesday, August 01, 2006			Sheet	31	of	36

SIO_GP20	SIO_GP21	V_DIMM
1	1	Normal
0	1	+50mV
1	0	+100mV
0	0	+150mV



平均分佈在POWER PLAN 和 PLAN 之間

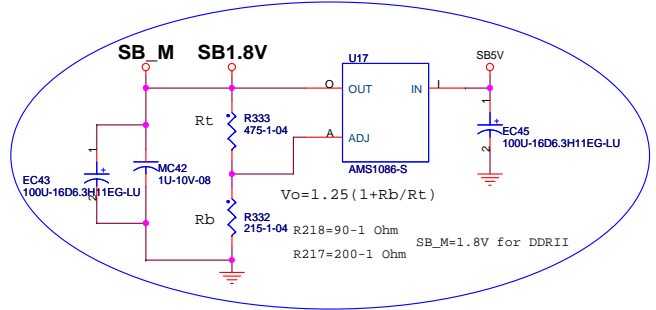
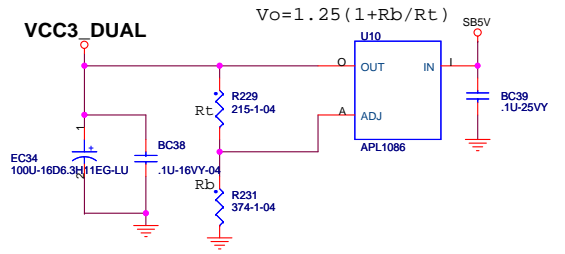
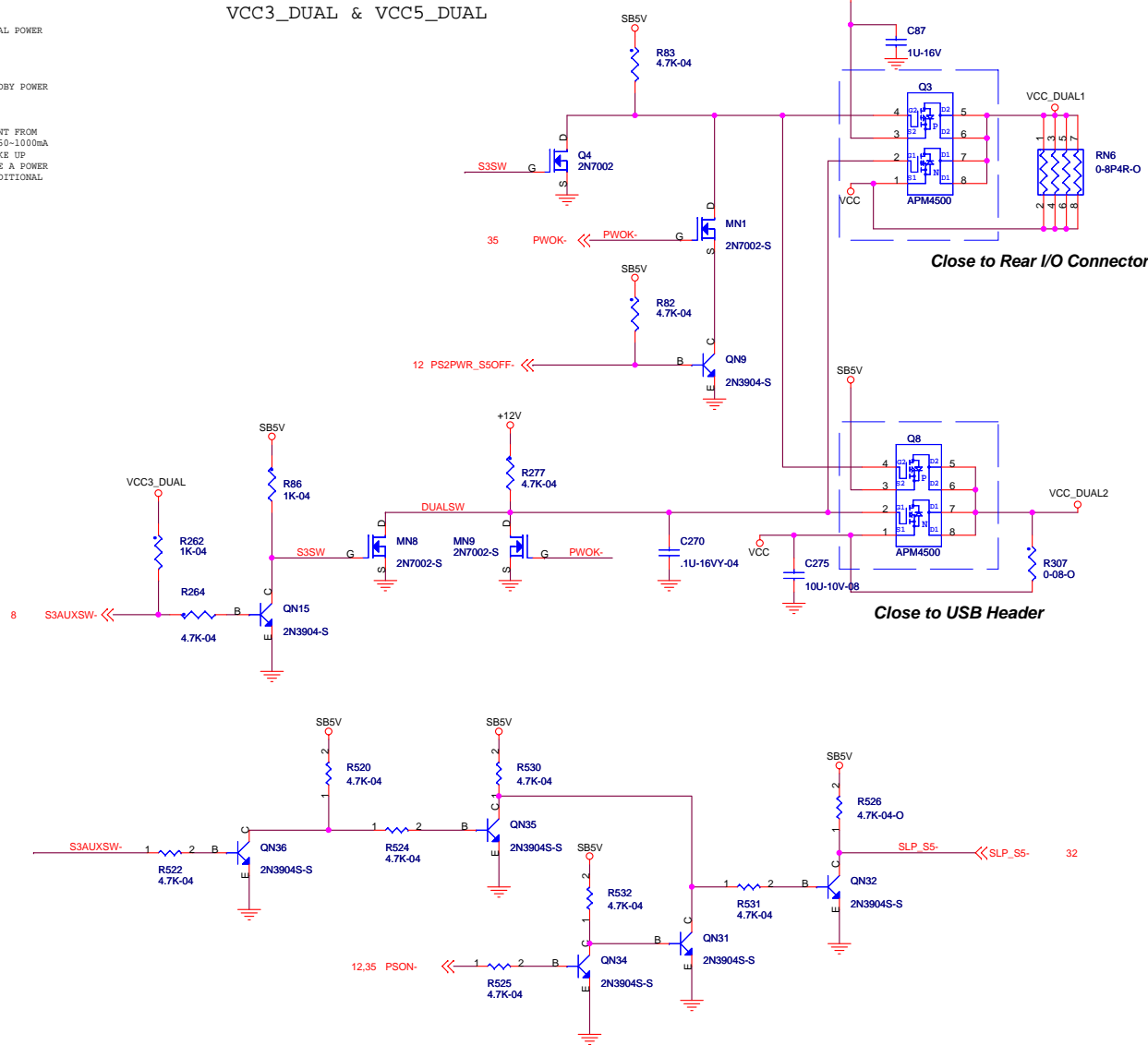
AUTO VOLTAGE SWITCH FOR ACPI STATE 3

1.IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER

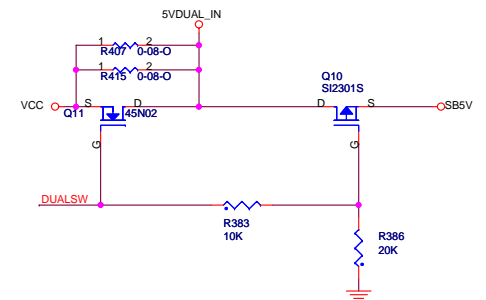
2.IN S3,S4,S5
THIS CIRCUIT PASSES THE STANDBY POWER

NOTE:
BECAUSE OF THE MAXIMUM CURRENT FROM
POWER SUPPLY IS ONLY ABOUT 750-1000mA
SO IF YOU WANT TO SUPPORT WAKE UP
FROM S3 BY USB, YOU MUST HAVE A POWER
SUPPLY WITH LARGER POWER. (ADDITIONAL
500mA PER USB PORT)

VCC3_DUAL & VCC5_DUAL

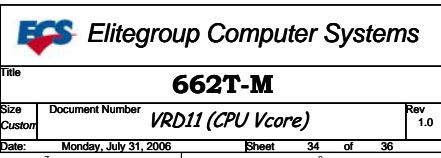


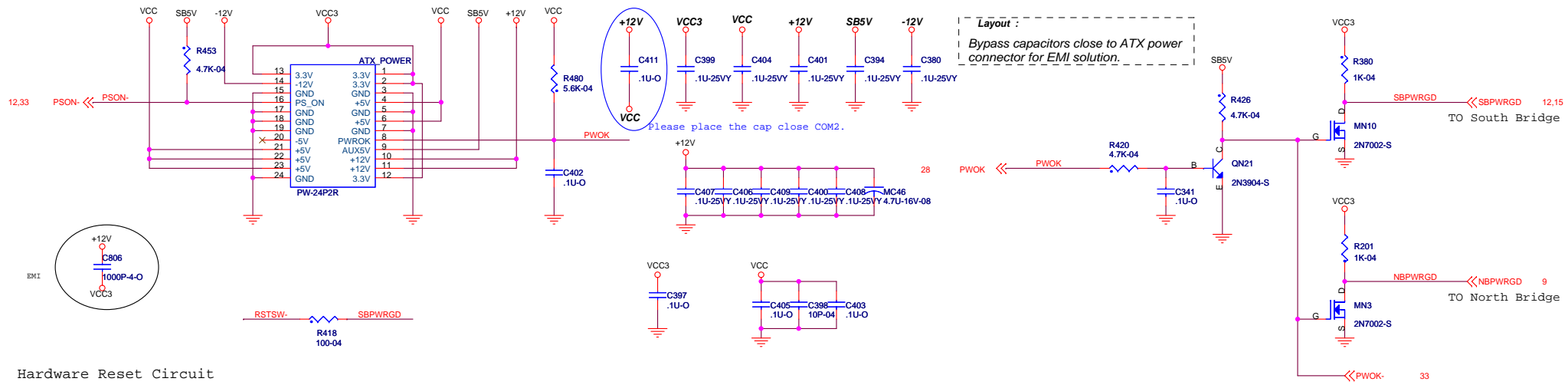
SB1.8V (For SB and DDRII) 800mA



Memory Power Output Control

	S3AUXSW-	PSON-	SLP_S5-
S0	1	0	1
S1	1	0	1
S3	0	1	1
S4	1	1	0
S5	1	1	0





Hardware Reset Circuit

FRONT PANEL

Intel Front Panel

For Acer

RTC

JP1	CLEAR CMOS
1-2	NORMAL
2-3	CLEAR

Del DD1(BAT54C)

Decoupling Capacitor

Place close to 963

Elitegroup Computer Systems

Title			662T-M
Size	Document Number	ATX / Panel / RTC	
Custom			
Date:	Friday, July 21, 2006	Sheet	35 of 36
Rev	1.0		

R1,R2,R3,R4 depend on the address selection.

ADD0	ADD1	ADDRESS
GND	GND	0x48
OPEN	GND	0x49
VCC	GND	0x4A
GND	OPEN	0x4B
OPEN	OPEN	0x4C
VCC	OPEN	0x4D
GND	VCC	0x4E
OPEN	VCC	0x4F
VCC	VCC	0x50

